Date Jan 31, 2023

Pin Type	Direction (*1)	Voltage Level	Description	Comments
General				
All pins				Applying a negative voltage or a voltage higher than the specified maximum, even for a short period of time, may damage the module permanently. The module does not have any protection against these hazards.
				The ESD protection level available on each module pin is module- and pin-specific. Enclustra recommends adding ESD protection circuitry to all signals connected to an externally-accessible connector.
				If FPGA/SoC/MPSoC chips have unbonded pins, tie those pins to GND or another defined potential to avoid floating copper.
User IO pins				
IO_P IO_N	Bidirectional	Bank-specific	FPGA I/O pin	Please check the supported IO standard's compatibility with the FPGA/SoC tools. Some banks may only have a restricted voltage range, e.g. 1.8 V.
				Some FPGA/SoC families have restrictions when LVDS and single-ended signals are placed on the same bank. The FPGA/SoC vendor provides further information. The best way to check your pinout is to perform a full compilation of the FPGA/SoC design using the vendor tools.
				Some user I/O pins may have additional functionalities, such as analog input or PCIe reset, or PUDC, or reference voltage input.
				Some modules may have unconnected pins.
				Some FPGA/SoC architectures may have higher capacitance on some pins (e.g. VREF) and therefore offer lower performance on these pins.
				Some modules may not support differential driver or receiver functionality on all of the IO_P/N pin pairs. They may only be usable for single ended I/O standards.
				Some FPGA/SoC families may not support terminating differential signals on all pin pairs inside the FPGA/SoC. External termination on the base board could be required. This may reduce the performance of such pairs due to the trace stubs slightly.
				Certain modules contain differential termination resistors on the module on some of the IO_P/N pin pairs. These terminations cannot be switched off. The IO_P pin could be used as single-ended I/O with limited performance. The IO_N pin should be tri-stated in the FPGA/SoC design.
				Most modules have pull-ups on all IO_P/N pins before and during configuration. These pull-ups cannot be switched off.
				The voltage on these pins may never exceed the voltage on the corresponding bank supply voltage. Check the FPGA/SoC data sheet for details.
			PUDC pin	Some modules have the pull-up-during-configuration pin exposed to the user connector. Some modules apply a 1 kOhm pull-down resistor during configuration (FPGA_DONE is low).
			Analog I/O pin	Some modules may have analog I/O functionality on some of the IO_P/N pins.
			System I/O pin	Some modules may have system peripheral pins on some of the IO_P/N pins. These pins usually cannot be driven from inside the programmable logic.
PCLK_P PCLK_N	Bidirectional	Bank-specific	Primary clock input	When designing a new module, we try to put global clock input pins on PCLK_P (if single-ended) or PCLK_P/N (if differential) pins.
				The use of PCLK_N as a single-ended clock may not be supported by some FPGA/SoC families.
				Some FPGA/SoC families may not support terminating differential signals on all pin pairs inside the FPGA/SoC. External termination on the base board could be required. This may reduce the performance of such pairs, due to the trace stubs slightly.
				Some FPGA/SoC families may not support using clock input pins as outputs.
			Other pin	On some modules, these pins may not be clock capable. In this case, refer to the description of the IO_P/N pin type.
SCLK_P SCLK_N	Bidirectional	Bank-specific	Secondary clock input	When designing a new module, we try to put any remaining clock input pins on SCLK_P (if single-ended) or SCLK_P/N (if differential) pins.
				Some of these clock pins may only be usable as regional clocks, restricting the location of synchronous elements within the FPGA/SoC.
				The use of SCLK_N as a single-ended clock may not be supported by some FPGA/SoC families.
				Some FPGA/SoC families may not support terminating differential signals on all pin pairs inside the FPGA/SoC. External termination on the base board could be required. This may reduce the performance of such pairs due to the trace stubs slightly.

				Some FPGA/SoC families may not support using clock input pins as outputs.
			Other pin	On some modules, these pins may not be clock capable. In this case, refer to the description of the IO_P/N pin type.
MGT_REFCLK_P MGT_REFCLK_N	Input or bidirectional	Bank-specific	Multi-gigabit-transceiver reference clock input (*2)	On modules supporting multi-gigabit-transceivers (MGT), the MGT_REFCLK_P/N pin pairs are reference clock inputs.
				Use AC coupling capacitors for connection to oscillator or to receiving device. The module does not contain any AC coupling capacitors on those signals.
				Check the FPGA/SoC vendors datasheet on specific requirements if unused.
			Other pin	On modules with less than the two MGT reference clock input pairs, these pins may be unconnected or regular FPGA/SoC I/Os. In this case, refer to the description of the IO_P/N pin type.
MGT_TX_P MGT_TX_N	Output or bidirectional	Bank-specific	Multi-gigabit-transceiver transmit output (*2)	On modules supporting MGTs, the MGT_TX_P/N pin pairs are the multi-gigabit-transceiver outputs.
				Use AC coupling capacitors for connection to oscillator or to receiving device. The module does not contain any AC coupling capacitors on those signals.
				Check the FPGA/SoC vendors datasheet on specific requirements if unused.
			Other pin	On modules with less than the maximum number of MGTs, these pins may be unconnected or regular FPGA/SoC I/Os. In this case, refer to the description of the IO_P/N pin type.
MGT_RX_P MGT_RX_N	Input or bidirectional	Bank-specific	Multi-gigabit-transceiver receive input (*2)	On modules supporting MGTs, the MGT_TX_P/N pin pairs are the multi-gigabit-transceiver inputs.
				Transmitter should be AC coupled to the receiver. The module does not contain any AC coupling capacitors on those signals.
				Check the FPGA/SoC vendors datasheet on specific requirements if unused.
			Other pin	On modules with less than the maximum number of MGTs, these pins may be unconnected or regular FPGA/SoC I/Os. In this case, refer to the description of the IO_P/N pin type.
JTAG pins				
JTAG_TDI JTAG_TMS JTAG_TDO JTAG_TCK	Input Input Output Input	Module-specific	JTAG chain, test data input JTAG chain, test mode select JTAG chain, test data output JTAG chain, test clock	The JTAG interface is available for FPGA/SoC configuration, debug and test.
				Most modules use VIN_CFG as the IO voltage for this interface.
				Enclustra recommends connecting these pins to a JTAG header as specified by the FPGA/SoC vendor.
				Enclustra recommends adding a 22 Ohm series termination resistor on the TCK signal and 100 Ohm series termination resistor on the other signals between the module and the JTAG header.
				Enclustra recommends adding low-capacitance (<5 pF) ESD protection diodes on the connector side of the series resistors close to the JTAG header.
				These pins have pull-ups / pull-downs as required by the FPGA/SoC on the module. Do not add additional pull-up / pull-down resistors.
				These pins may be left floating.
I2C pins				
I2C_SCL I2C_SDA I2C_INT#	Bidirectional, Open Drain	3.3 V	I2C bus, clock I2C bus, data I2C bus, interrupt, active-low	All modules have a I2C bus that is available for use on the baseboard.
				All signals are open drain. The modules already contain pull-ups on these pins.
				When adding additional peripherals to this bus, make sure that there is no address conflict.
				Do not drive these pins to a logic high level. Only allow these signals to be driven low.
				I2C_INT# can only be used as an input to the FPGA/SoC, not as an output from the FPGA/SoC.
				100 Ohm series resistors should be added between the module and I2C device on the base board when the I2C traces are long.
Flash SPI pins				
FLASH_CLK FLASH_DI FLASH_DO FLASH_CS#	Bidirectional	Module-specific	Flash SPI bus, clock input Flash SPI bus, data input Flash SPI bus, data output Flash SPI bus, chip select input, active-low	On most modules, the SPI Flash and the FPGA/SoC are connected to these pins.
				Most modules use VIN_CFG as the IO voltage for this interface.
				This signal group is available to the base board as a way to access the SPI Flash from the base board.

				For modules equipped with a Quad SPI Flash, only the 1- or 2-bit commands are usable from the base board, as the upper IO bits (IO2, IO3) are not available on the module connector.
				Most FPGA/SoC modules also support the slave serial programming through the FLASH_CLK and FLASH_DO or FLASH_DI pins.
				It is important that all possible drivers on the base board are tristated before the FPGA/SoC is driving onto the Flash SPI signals.
				Enclustra recommends to pull POR#_LOAD# low while accessing the SPI Flash from the base board.
				If the module contains level shifters between these pins and the SPI flash and/or the FPGA/SoC, the FLASH_DO pin may always be driven out of the module, even though FLASH_CS# is high.
				The FPGA/SoC accesses the SPI Flash either for booting, from a SPI controller inside the FPGA/SoC design, or from a SoC peripheral.
				These pins have 2.2 kOhm to 10 kOhm pull-ups on the module. Do not add additional pull-up / pull-down resistors on the base board. The pull-ups are connected to either VIN_CFG or the 3.3 V rail. Make sure that components connected to these pins on the base board are 3.3 V-tolerant, or have clamp diodes to VIN_CFG.
				The Flash SPI clock signal (FLASH_CLK) should be routed short (< 50 mm) and stub-less on the base board, adding a maximum of 15 pF of load capacitance including trace capacitance.
				All Flash SPI signals run at high speeds. Use an adjacent ground plane when using these signals on the base board to prevent EMC issues.
				These pins may be left floating.
Configuration pins				
BOOT_MODE	Bidirectional	Module-specific	Boot-mode selection	This pin selects between different module-specific boot modes, if supported.
				Most modules use VIN_CFG as the IO voltage for this interface.
				This pin has a 2.2 kOhm to 10 kOhm pull-up on the module. The pull-up is connected to either VIN_CFG or the 3.3 V rail. Make sure that components connected to this pin on the base board are 3.3 V tolerant or have a clamp diode to VIN_CFG.
				For a BOOT_MODE of '1', leave this pin floating or use a 1 kOhm to 10 kOhm pull-up resistor.
				For a BOOT_MODE of '0', add a 470 Ohm to 680 Ohm pull-down resistor.
				The USB device controller available on some modules and on some Enclustra base boards is also able to drive onto this pin. For best interoperability, do not connect this pin to GND without the recommended series resistor.
				On modules equipped with a Microchip FPGA/SoC this pin does not have a special function. This pin can be used as a normal I/O.
POR#_LOAD#	Bidirectional, Open Drain	Module-specific	Power-on-reset or configuration-clear input, active-low	The POR#_LOAD# signal is used as a power-up-reset (POR_B, nPOR) input on SoC modules.
				The POR#_LOAD# signal is used as a configuration load signal input (nCONFIG, PROG_B) on FPGA modules.
				Most modules use VIN_CFG as the IO voltage for this interface.
				Mars only: This pin should be driven low after power-on until some FPGA/SoC-specific time after all VIN_IO, VIN_CFG and VIN_3V3 power inputs are stable. Either a voltage supervisor device or a buffered PWR_GOOD signal from these respective power converters on the base board should be connected to this pin using an open drain circuit.
				Mercury only: This pin should be driven low after power-on until some FPGA/SoC-specific time after all VIN_IO and VIN_CFG power inputs are stable. Either a voltage supervisor device or a buffered PWR_GOOD signal from these respective power converters on the base board should be connected to this pin using an open drain circuit.
				A minimum delay of 10 ms from the assertion of PWR_GOOD to the release of the POR#_LOAD# signal is required.
				This pin should only be left floating, if after power-on all power inputs rise to the specified voltage level within a time period shorter than the FPGA/SoC-specific start delay.
				Enclustra recommends adding a push-button to ground on this pin.
				The module contains a 2.2 kOhm to 10 kOhm pull-up on this signal. Do not add additional pull-up / pull-down resistors. The pull-up is connected to either VIN_CFG or the 3.3 V rail. Make sure that components connected to this pin on the base board are 3.3 V-tolerant or have a clamp diode to VIN_CFG.
				Do not drive this pin to a logic high level. Only allow this signal to be driven low.
				This pin should be driven low when the power source is disconnected or switched off. Unexpected side-effects may occur if the module is operated outside the specified voltage levels (EEPROM corruption, Flash corruption, etc.).
				Some modules contain over-voltage protection circuits for VIN_IO supplies. When an over-voltage is detected, this pin is driven low.

SRST#_RDY#	Bidirectional, Open Drain	Module-specific	Soft-reset or configuration-delay signal, active-low	The SRST#_RDY# signal is used as a soft-reset (nRST, SRST) input on SoC modules.
				The SRST#_RDY# signal is used as a configuration ready output and configuration delay input (INIT_B, nSTATUS) on FPGA modules.
				Most modules use VIN_CFG as the IO voltage for this interface.
				Enclustra recommends connecting this signal to the JTAG connector for SoC processor debugging.
				Do not drive this pin to a logic high level. Only allow this signal to be driven low.
				The module contains a 2.2 kOhm to 10 kOhm pull-up on this signal. Do not add additional pull-up / pull-down resistors. The pull-up is connected to either VIN_CFG or the 3.3 V rail. Make sure that components connected to this pin on the base board are 3.3 V tolerant or have a clamp diode to VIN_CFG.
				This pin may be left floating.
				On modules equipped with a Microchip FPGA/SoC this pin is not used as a soft-reset as described above but as a programming mode configuration pin. Refer to the module's user manual for more information about the usage of this pin.
FPGA_DONE	Output	Module-specific	Configuration done output, active-high	The FPGA_DONE pin is an output and indicates whether the FPGA/SoC design has been loaded successfully.
				Most modules use VIN_CFG as the IO voltage for this pin.
				This pin may be left floating.
				Enclustra recommends using a transistor or logic buffer to drive a status LED. Use a 10 kOhm to 47 kOhm pull-down to prevent this signal from floating when no module is installed. The source impedance of this pin is between 330 Ohm and 1000 Ohm.
				Do not drive onto this pin on the base board.
				On modules equipped with a Microchip FPGA/SoC this pin does not have a special function. This pin can be used as a normal I/O.
RSVD	Module-specific	Module-specific	Miscellaneous use, i.e. analog input, boot mode, external clock input	Refer to the module's user manual for more information about the usage of these pins.
				On some modules pin A-110 is reserved for VBUS_DETECT. This pin must be connected to the VBUS pin of the USB connector on the base board (not to the USB_VBUS input pin of the module) via a voltage divider consisting of 2 resistors of 1 kOhm each .
USB pins				
USB_DP USB_DM	Bidirectional	USB standard	USB device, host or OTG signal pin pair	The USB pin group contains a module-specific USB interface, if available. It can be a USB 2.0 or 3.0 device, a USB 2.0 host or a USB 2.0 OTG (host/device) interface.
				The USB pin group may be left floating if the USB interface is not used.
				In device mode, the USB_DP/DM pin pair is used to connect the module to a host computer.
				In host mode, the USB_DP/DM pin pair is used to connect the module with a USB peripheral.
				Enclustra recommends connecting the USB_DP/DM pins to a USB B-type (device) or A-type (host) or AB-type (OTG) receptacle.
				Enclustra recommends adding low-capacitance (<= 1 pF) ESD protection diodes close to the USB connector.
VBUS_HDP	Input or bidirectional	Module-specific, 5V or USB Standard	Common	Refer to the module's user manual for more information about the usage of these pin.
			USB host signal	The HDP/HDM pin pair is used to connect the module with a USB peripheral.
				Enclustra recommends connecting the HDP/HDM pins to a A-type (host) receptacle.
				Enclustra recommends adding low-capacitance (<= 1 pF) ESD protection diodes close to the USB connector.
				This pin may be left floating if the USB interface is not used.
			OTG VBUS detect input	The VBUS signal is used to detect USB power.
				The module does not draw power from this pin.
				This pin may be left floating if the USB interface is not used.
ID_HDM	Input or bidirectional	USB standard	Common	Refer to the module's user manual for more information about the usage of these pin.
			USB host signal	The HDP/HDM pin pair is used to connect the module with a USB peripheral.
				Enclustra recommends connecting the HDP/HDM pins to a A-type (host) receptacle.
				Enclustra recommends adding low-capacitance (<= 1 pF) ESD protection diodes close to the USB connector.
				This pin may be left floating if the USB interface is not used.
			USB OTG ID input	In USB 2.0 OTG mode, the ID pin is used to detect if a host or a device has been connected. Connect it to the AB-type USB connector.
				In USB 2.0 or USB 3.0 device mode, this pin should be left floating. The ID pin of the USB connector (if any) should be left floating.
				In USB 2.0 host mode, this pin should be connected to GND. The ID pin of the USB connector (if any) should be connected to GND.

				This pin may be left floating.
USB_CPEN	Output	3.3 V	USB VBUS enable output, active-high	In USB 2.0 OTG mode, the USB_CPEN pin is used to enable the VBUS load switch on the base board to enable bus-power to the connected USB device.
				In USB 2.0 host and USB 2.0 OTG mode, Enclustra recommends to use a USB-type active-high load switch on the base board between a 5 V power supply and USB_VBUS. Add >= 120 uF (host) or 10 uF (OTG) of capacitance on the USB connector-side of the load switch as per the USB standard.
				This pin may be left floating.
USB_SSRX_P USB_SSRX_N (Mercury only)	Input	USB standard	USB 3.0 super-speed receive pair	The USB_SSRX_P/N pin pair is used as a 5.0 Gbps receive data pair in USB 3.0 device applications, for modules that are equipped with a USB 3.0 device controller. These connections are not used by Mercury XU* modules (Zynq Ultrascale+ modules with Xilinx built-in USB 3.0 support use MGT GTR lines for USB 3.0 interface).
				Enclustra recommends adding low-capacitance (<0.5 pF) ESD protection devices on this pin pair.
				A solid ground plane, a maximum of two vias and high-speed routing guidelines need to be observed carefully.
				The nominal differential impedance of this signal pair is 90 Ohm.
				This pin pair may be left floating for non-USB 3.0 applications.
USB_SSTX_P USB_SSTX_N (Mercury only)	Output	USB standard	USB 3.0 super-speed transmit pair	The USB_SSTX_P/N pin pair is used as a 5.0 Gbps transmit data pair in USB 3.0 device applications, for modules that are equipped with a USB 3.0 device controller. These connections are not used by Mercury XU* modules (Zynq Ultrascale+ modules with Xilinx built-in USB 3.0 support use MGT GTR lines for USB 3.0 interface).
				Enclustra recommends adding low-capacitance (<0.5 pF) ESD protection devices on this pin pair.
				A solid ground plane, a maximum of two vias and high-speed routing guidelines need to be observed carefully.
				The nominal differential impedance of this signal pair is 90 Ohm.
				This pin pair may be left floating for non-USB 3.0 applications.
Ethernet				
All Ethernet pins				These pins may be left floating if the Ethernet interface(s) is/are not used. Enclustra recommends pulling the reset signal of the Ethernet PHY low to reduce power consumption.
ETHx_A_P ETHx_A_N	Bidirectional	Ethernet standard	Gigabit Ethernet pair A	For modules with a Gigabit Ethernet PHY on these pins, these pins should be connected to the A pin pair (1=P, 2=N) of the RJ45 connector via suitable Gigabit Ethernet magnetics.
	Output		Fast Ethernet lower channel transmit pair	For modules with a Fast Ethernet PHY on these pins, these pins should be connected to the TX pin pair (1=P, 2=N) of the lower channel RJ45 connector via suitable Fast or Gigabit Ethernet magnetics.
ETHx_B_P ETHx_B_N	Bidirectional	Ethernet standard	Gigabit Ethernet pair B	For modules with a Gigabit Ethernet PHY on these pins, these pins should be connected to the B pin pair (3=P, 6=N) of the RJ45 connector via suitable Gigabit Ethernet magnetics.
	Input		Fast Ethernet lower channel receive pair	For modules with a Fast Ethernet PHY on these pins, these pins should be connected to the RX pin pair (3=P, 6=N) of the lower channel RJ45 connector via suitable Fast or Gigabit Ethernet magnetics.
ETHx_C_P ETHx_C_N	Bidirectional	Ethernet standard	Gigabit Ethernet pair C	For modules with a Gigabit Ethernet PHY on these pins, these pins should be connected to the C pin pair (4=P, 5=N) of the RJ45 connector via suitable Gigabit Ethernet magnetics.
	Output		Fast Ethernet upper channel transmit pair	For modules with a Fast Ethernet PHY on these pins, these pins should be connected to the TX pin pair (1=P, 2=N) of the upper channel RJ45 connector via suitable Fast or Gigabit Ethernet magnetics.
ETHx_D_P ETHx_D_N	Bidirectional	Ethernet standard	Gigabit Ethernet pair D	For modules with a Gigabit Ethernet PHY on these pins, these pins should be connected to the D pin pair (7=P, 8=N) of the RJ45 connector via suitable Gigabit Ethernet magnetics.
	Input		Fast Ethernet upper channel receive pair	For modules with a Fast Ethernet PHY on these pins, these pins should be connected to the RX pin pair (3=P, 6=N) of the upper channel RJ45 connector via suitable Fast or Gigabit Ethernet magnetics.
ETHx_LED1#	Output	3.3 V	Ethernet LED 1, active low	Most modules indicate link activity on this signal.
				Enclustra recommends connecting this signal to a yellow LED on the RJ45 connector with a 150 Ohm series resistor to VCC_3V3.
				Do not add pull-up or pull-down resistors on this pin. Do not drive onto this pin.
				This pin may be left floating if not used.
ETHx_LED2#	Output	3.3 V	Ethernet LED 2, active low	Most modules indicate link status on this signal.
				Enclustra recommends connecting this signal to a green LED on the RJ45 connector with a 150 Ohm series resistor to VCC_3V3.
				Do not add pull-up or pull-down resistors on this pin. Do not drive onto this pin.
				This pin may be left floating if not used.
ETHx_CTREF	Output	Module-specific	Ethernet magnetics center tap power output	For modules with the SMSC LAN8710Ai or TI TLK105 Fast Ethernet PHYs, connect this signal to the four center taps of the Ethernet magnetics and attach a 1 uF (10 V) capacitor to every center tap pin as per the PHY datasheet. Ethernet Magnetics (maybe integrated into a RJ45 connector) where the four center taps are interconnected can be used.

				For modules with the Micrel KSZ9021 or KSZ9031 Gigabit Ethernet PHY, do NOT connect this signal to the four center taps of the Ethernet magnetics. Only Ethernet magnetics (maybe integrated into a RJ45 connector) with separate center tap pins for each pair should be used. Attach a 1 uF (10 V) capacitor to every center tap pin as per the PHY data sheet.
				For best compatibility between current and future modules, Enclustra recommends using a circuit using five MOSFET transistors as implemented on the Mercury PE1 and Mars EB1 base boards.
				Other implementations (Mars Starter, Mars PM3, Mercury Starter) are not optimal and are not recommended. In particular, interconnecting the A/B and C/D pin pair center taps when operating the Micrel Gigabit PHYs in Fast Ethernet mode leads to significantly higher power consumption.
Power pins				
VIN_MOD	Power Input	5-15V +-5% (Mercury only (*3)) 3.3-5V +-5% (Mars only)	Module power input	This pin needs to be connected to an adequate power supply on the base board.
				Enclustra recommends a voltage rise time of <10 ms after power-on. If the voltage rise time is longer, keep PWR_EN low until the supply voltage is in the valid range.
				Some modules may accept lower or higher input voltages. Please contact Enclustra.
				POR#_LOAD# should be driven low when this power input is below the specified voltage range.
				Enclustra recommends adding reverse and over-voltage protection circuitry on the base board.
				Enclustra recommends a maximum voltage ripple of +-3% of the average value on this pin.
				The module does not require power-sequencing between VIN_MOD and VIN_3V3.
				Enclustra recommends at least 100 uF of capacitance on the base board on this power rail.
VIN_IO	Power Input	Bank-specific	User I/O bank power input	This pin needs to be connected to an adequate power supply on the base board.
				Please check the voltage range supported by the connected FPGA/SoC. Some banks may only have a restricted voltage range.
				Enclustra recommends a voltage rise time of <10 ms after power-on.
				Each bank of each module has a range of allowed I/O voltages.
				POR#_LOAD# should be driven low when this power input is below the specified voltage range.
				Check the FPGA/SoC vendors datasheet for specific power requirements (ripple, noise).
				Check the FPGA/SoC vendors datasheet for power sequencing requirements.
				These pins may also be connected to peripherals on some modules. Please make sure you power this pins even if you don't use the user I/Os of this bank on the base board.
				No power should be applied to this pin when VIN_MOD and VIN_3V3 (Mars only) are not within operating range. Connecting VOUT to VIN_IO is allowed.
				Connecting 3.3 V to VIN_IO may require power sequencing using a load switch or P-channel MOSFET. Check the FPGA/SoC datasheet for power sequencing details.
				No power should be applied to this pin when VIN_MOD and VIN_3V3 (Mars only) are not within operating range. Check the FPGA/SoC datasheet for power sequencing details.
				Enclustra recommends a 1 uF (10 V) capacitor on the base board per pin.
VIN_CFG	Power Input	Module-specific	Configuration bank power input	These pins needs to be connected to an adequate power supply on the base board.
				Enclustra recommends a voltage rise time of <10 ms after power-on.
				Each module has a range of allowed configuration bank voltages.
				These pins may also be connected to User I/O banks.
				POR#_LOAD# should be driven low when this power input is below the specified voltage range.
				Check the FPGA/SoC vendors datasheet for specific power requirements (ripple, noise).
				Check the FPGA/SoC vendors datasheet for power sequencing requirements.
				These pins may also be connected to peripherals on some modules.
				No power should be applied to this pin when VIN_MOD and VIN_3V3 (Mars only) are not within operating range. Connecting VOUT to VIN_IO is allowed.
				Connecting 3.3 V to VIN_IO may require power sequencing using a load switch or P-channel MOSFET. Check the FPGA/SoC datasheet for power sequencing details.
				No power should be applied to this pin when VIN_MOD and VIN_3V3 (Mars only) are not within operating range. Check the FPGA/SoC datasheet for power sequencing details.
				Enclustra recommends a 1 uF (10 V) capacitor on the base board per pin.
VIN_3V3 (Mars only)	Power Input	3.3 V +-5%	Module power input	This pin needs to be connected to an adequate power supply on the base board.
				Enclustra recommends a voltage rise time of <10 ms after power-on.

				Some modules may accept lower or higher input voltages. Please contact Enclustra.
				POR#_LOAD# should be driven low when this power input is below the specified voltage range.
				Enclustra recommends a maximum voltage ripple of +-3% of the average value on this pin.
				The module does not require power-sequencing between VIN_MOD and VIN_3V3.
				If required by the FPGA/SoC, the module performs the necessary power sequencing.
				Enclustra recommends at least 22 uF of capacitance on the base board on this power rail.
VOUT_3V3 (Mercury only)	Power Output	3.3 V +-5%	Module power output	The 3.3 V power converter on the module is enabled irrespective of the level on PWR_EN.
				The maximum power that can be drawn is 300 mA per pin.
				Please verify that the power capability of each power converter on the module is not exceeded.
				When not used, these pins may be left floating or connected via a 0.1 to 1 uF (10 V) capacitor to GND for slightly better performance of the neighboring signal pins.
VOUT	Power Output	Module-specific	Power output with module specific output voltage.	Each pin is connected to a module-specific power converter output.
				The maximum power that can be drawn is 300 mA per pin.
				Do not connect these pins to a power source on the base board.
				Please verify that the power capability of each power converter on the module is not exceeded.
				For best migration between modules, do not use this power output on the base board. Add an optional 0.1 to 1 uF (10 V) capacitor to GND with a maximum trace length of 3 mm for best signal integrity of adjacent signal pairs when used at speeds >100 Mbps.
				When not used, these pins may be left floating or connected via a 0.1 to 1 uF (10 V) capacitor to GND for slightly better performance of the neighboring signal pins.
VIN_BAT	Power Input	Module-specific	Battery power input	This pin connects to the real-time clock if available on the module.
				This pin connects also to the FPGA/SoC encryption key battery backup pin on some modules.
				Use a Schottky diode and a 10 kOhm to 47 kOhm series resistor between the battery on the base board and this pin. The diode is required because some modules may source power to this pin from a rechargeable battery.
				When not using a battery on the base board, leave this pin floating.
GND	Ground		Ground	On the base board, connect these pins to a ground plane with wide and very short traces.
Power control and status pins				
PWR_EN	Input, Open Drain	3.3 V	Power enable, active-high	By pulling this pin low, some power converters on the module are disabled. This pin can be used for power sequencing or to save power.
				When pulling this pin low, all volatile configuration data and memory contents are lost and all User I/O pins go to a high impedance state.
				This pin should be driven low on the base board when the VIN_MOD power input is below the specified voltage range. Usually, the power good signal of the VIN_MOD source should be connected to this pin.
				The module contains a 2.2 kOhm to 10 kOhm pull-up to VIN_3V3 (Mars)/VOUT_3V3 (Mercury) on this pin. A pull-up on the base board is not needed.
				Mars only: Make sure that the VIN_3V3 power converter on the base board is not disabled by a logic low level on this pin. This would lead to a deadlock since the pull-up depends on the 3.3 V supply for proper operation.
				This pin may be left floating.
PWR_GOOD	Output, Open Drain	3.3 V	Power good, active-high	The module contains a 2.2 kOhm to 10 kOhm pull-up to VIN_3V3 (Mars)/VOUT_3V3 (Mercury) on this pin. A pull-up on the base board is not needed.
				Some of the module's power converters pull this pin low when their output voltage is below a power good threshold.
				Mars only: Make sure that the VIN_3V3 power converter on the base board is not disabled by a logic low level on this pin. This would lead to a deadlock since the pull-up depends on the 3.3 V supply for proper operation.
				This pin may be left floating.
VMON	Output	Module-specific	Voltage monitoring output	These pins are used for module production test only.
				No power may be drawn from these pins.
				Leave these pins floating or connected via a 0.1 to 1 uF (10V) capacitor to GND for slightly better performance of the neighboring signal pins. A direct connection to GND is also permitted.
C_PRSNT#	Input	3.3 V	Module connector C detection pin	Must be connected to GND on the base board. Depending on the value of this pin, the FPGA/SoC banks on the C connector of the Mercury+ module are supplied with the voltages provided by the user (C_PRSNT# low) or with default voltages (C_PRSNT# n.c. and pulled up internally on the Mercury+ module).

Notes:
1. Direction of signal pin is as seen from the module.

2. On modules with Microchip Polarfire FPGAs/SoCs MGTs are called XCVRs
3. The range of VIN_MOD is limited to 5-13.2V +-5% for ME-MP1 modules

Disclaimers:
All pinout and pin information is provided as-is without assurance of correctness or completeness.
All information is subject to change at any time without notice.
Please verify all data with Enclustra's user manuals, FPGA and other components vendor's documentation.
Enclustra recommends checking the module's and the FPGA and other components errata sheets.