Mercury+ PE1 Base Board

User Manual

Purpose

The purpose of this document is to present the characteristics of Mercury+ PE1 base board to the user, and to provide the user with a comprehensive guide to understanding and using the Mercury+ PE1 base board.

Summary

This document first gives an overview of the Mercury+ PE1 base board followed by a detailed description of its features and configuration options. In addition, references to other useful documents are included.

Product Information	Code	Name
Product	ME-PE1	Mercury+ PE1 Base Board

Document Information	Reference	Version	Date
Reference / Version / Date	D-0000-423-001	06	25.05.2020

Approval Information	Name	Position	Date
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Document History

Version	Date	Author	Comment
06	25.05.2020	DIUN, HMEY	Added information on R4.6 boards and system controller firmware, corrected default settings for the voltage jumpers and DIP switches, added information on mPCIe support for Zynq Ultrascale+ modules
05	08.01.2019	DIUN	Updated sections about USB and clock generator, other minor corrections
04	05.05.2017	DIUN	Minor corrections and clarifications, updated dimensions
03	26.08.2016	DIUN	Version 03, updated dimensions information
02	30.06.2016	DIUN	Version 02, added FMC pinout information
01	24.03.2016	DIUN	Version 01 (without system controller)

Table of Contents

1 Overview

1.1 General

1.1.1 Introduction

The Mercury+ PE1 base board is equipped with a multitude of I/O interfaces for use with Mercury family FPGA and SoC modules. The board is well-suited for rapid prototyping and for building FPGA systems, without the need for developing custom hardware.

The board can also be used for production flash programming on Mercury modules, or for educational purposes.

The main features of the Mercury+ PE1 base board are:

- Support for USB 3.0 device and USB 2.0 host
- FTDI USB 2.0 High-Speed device controller
- PCIe Gen2 ×4 interface
- High-speed FPGA and flash programming over USB
- Support for USB 3.0 to FPGA communication
- High-bandwidth and seamless operation with optional Enclustra FPGA Manager IP Solution [2]
- Differential signal pairs available on the module connector fit for various high-speed I/O applications
- I/O interfaces for a wide range of applications
- Industry-standard FMC connector (LPC, HPC or 2 ×LPC, depending on the board variant)
- mPCIe and mSATA support for integration of storage, GSM, UMTS and other interface cards
- microSD card slot
- Simple integration by using a single 12 V voltage supply (standalone configuration)
- Alternative power supply over PCIe connector (PCIe configuration)
- Alternative power supply via USB device port

1.1.2 Warranty

Please refer to the General Business Conditions, available on the Enclustra website [1].

1.1.3 RoHS

The Mercury+ PE1 base board is designed and produced according to the Restriction of Hazardous Substances (RoHS) Directive (2011/65/EC).

1.1.4 Disposal and WEEE

The Mercury+ PE1 base board must be properly disposed of at the end of its life. If a battery is installed on the board, it must also be properly disposed of.

The Waste Electrical and Electronic Equipment (WEEE) Directive (2002/96/EC) is not applicable for the Mercury+ PE1 base board.

1.1.5 Safety Recommendations and Warnings

Mercury boards are not designed to be "ready for operation" for the end-user. Proper configuration of the hardware before usage is required.

Ensure that the power supply is disconnected from the board before inserting or removing a Mercury module, connecting interfaces, or connecting jumpers.

Touching the capacitors of the DC-DC converters can lead to voltage peaks and permanent damage; over-voltage on power or signal lines can also cause permanent damage to the board and to the equipped module.

Warning!

It is possible to mount some Mercury modules the wrong way round on the Mercury+ PE1 base board - always check that the mounting holes on the base board are aligned with the mounting holes of the module.

The base board and module may be damaged if the module is mounted the wrong way round and powered up.

Warning!

Certain older revisions of the Mercury KX1 FPGA module cannot be used in combination with Mercury+ base boards (with three module connectors), due to a mechanical collision caused by large capacitors on the bottom side of the module.

Always check that the mounting holes on the base board are aligned with the mounting holes of the Mercury+ PE1 base board. If the module cannot be mounted correctly due to the mechanical collision, please contact Enclustra support.

1.1.6 Electrostatic Discharge

Electronic boards are sensitive to electrostatic discharge (ESD). Please ensure that the product is handled with care and only in an ESD-protected environment.

1.1.7 Electromagnetic Compatibility

The Mercury+ PE1 base board is a Class A product and is not intended for use in domestic environments. The product may cause electromagnetic interference, for which appropriate measures must be taken.

1.2 Deliverables

- Mercury+ PE1 base board including bracket and plastic standoffs
- Mercury+ PE1 base board documentation, available via download:
  - Mercury+ PE1 Base Board User Manual (this document)
  - Mercury+ PE1 Base Board IO Net Length Excel Sheet [3]
  - Mercury+ PE1 Base Board User Schematics (PDF) [4]
  - Mercury+ PE1 Base Board Known Issues and Changes [5]
  - Mercury+ PE1 Base Board 3D Model (PDF) [6]
  - Mercury+ PE1 Base Board STEP 3D Model [7]
  - Module Pin Connection Guidelines [8]
  - Mercury Master Pinout [9]

1.3 Accessories

- Mercury/Mercury+ FPGA or SoC module
- 12 V DC/1.5 A power supply
- USB 2.0 A to micro-B USB cable

2 Getting Started

This section contains essential information on using the Mercury+ PE1 base board.

Before first use of the Mercury+ PE1 base board with a Mercury or Mercury+ module, the following steps must be followed:

- Mount the module on the module slot on the base board, with the power switched off.

  It is possible to mount some Mercury modules the wrong way round on the Mercury+ PE1 base board - always check that the mounting holes on the base board are aligned with the mounting holes of the module.

  The base board and module may be damaged if the module is mounted the wrong way round and powered up.

  Warning!

  Certain older revisions of the Mercury KX1 FPGA module cannot be used in combination with Mercury+ base boards (with three module connectors), due to a mechanical collision caused by large capacitors on the bottom side of the module.

  Always check that the mounting holes on the base board are aligned with the mounting holes of the Mercury+ PE1 base board. If the module cannot be mounted correctly due to the mechanical collision, please contact Enclustra support.

- Set the DIP switches correctly (refer to Section 6.3).
- Set the I/O voltage selection jumpers correctly (refer to Section 5.7).
- Power up the board (refer to Section 5 for power options).

The power supply of the base board must be turned off in the following situations:

- Before changing the position of the I/O voltage selection jumpers
- Before removing the Mercury or Mercury+ module
- Before connecting or disconnecting peripherals to ANIOS and I/O connectors
- Before connecting or disconnecting FMC cards

Before connecting peripherals, make sure that the corresponding VCC_IO voltage is properly set.

The operating conditions for the Mercury+ PE1 base board and equipped module must conform to the values given in Section 7, and in the relevant section from the Mercury or Mercury+ module user manual.

Warning!

The Mercury+ PE1 base board can only be used in combination with a Mercury or Mercury+ module. Using the board without module will cause the "FAIL" LED to turn on; refer to Section 6.1 for details.

3 Board Description

3.1 Block Diagram

The Mercury+ PE1 base board is available in three different hardware configurations:

- PE1-200 (low cost, ideal in combination with Mercury modules; 1 × FMC LPC connector)
- PE1-300 (high flexibility, ideal in combination with Mercury+ modules due to the third module connector; 1 × FMC HPC connector)
- PE1-400 (high flexibility, ideal in combination with Mercury+ modules due to the third module connector; 2 × FMC LPC connectors)

All Mercury+ PE1 base board variants can be used in combination with all Mercury or Mercury+ modules. In order to have a higher number of I/Os routed from the module to the base board, it is recommended to use a Mercury+ module with PE1-300/400 board variants.

Table 1 describes the features of the Mercury+ PE1 base board for all variants.

The block diagrams of each configuration are shown in Figures 1, 2 and 3.

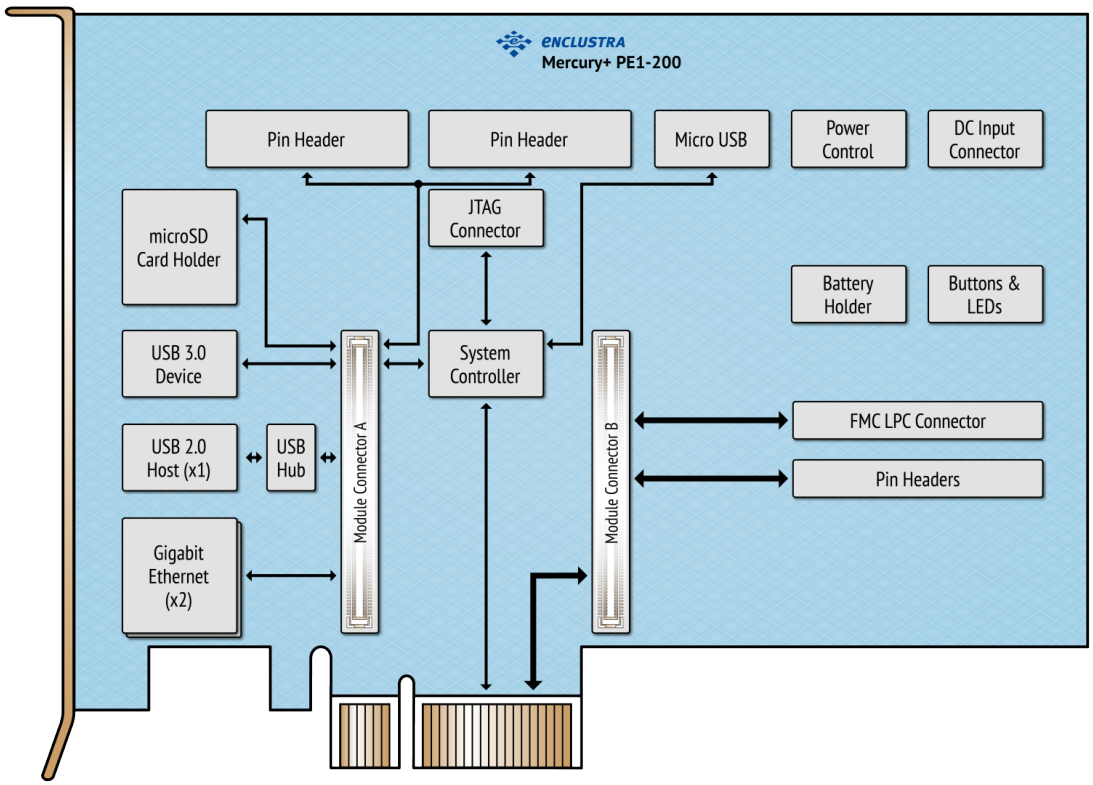

Figure 1: Hardware Block Diagram PE1-200

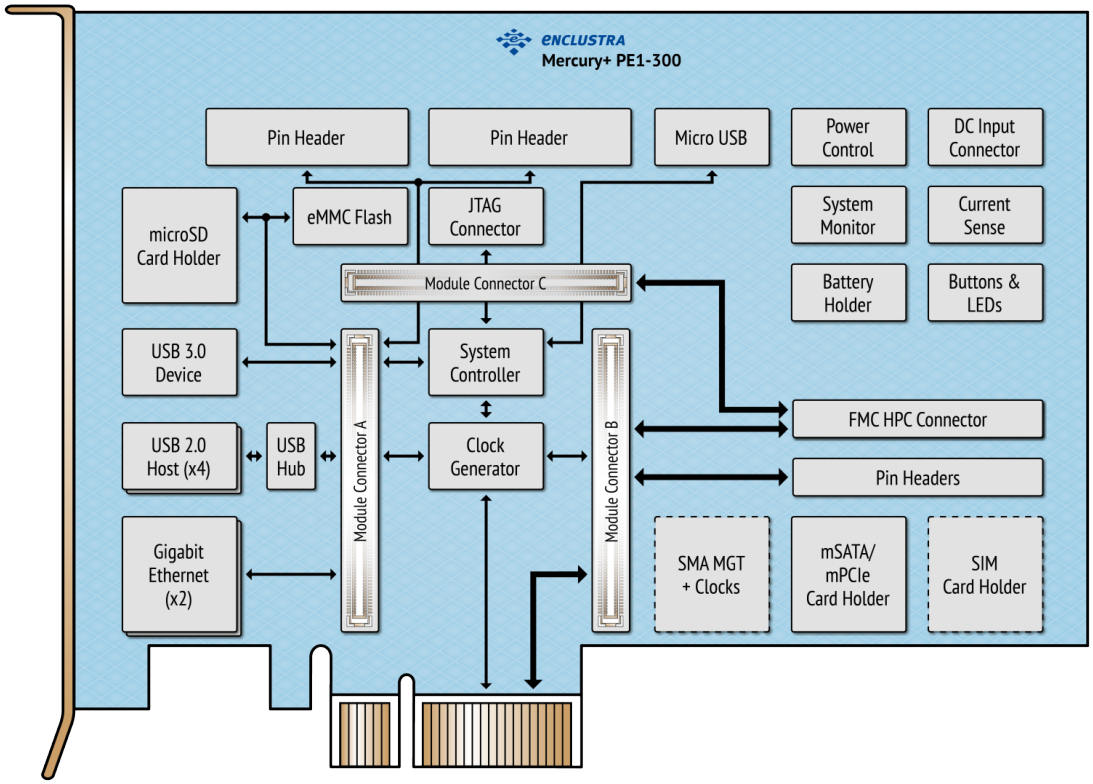

Figure 2: Hardware Block Diagram PE1-300

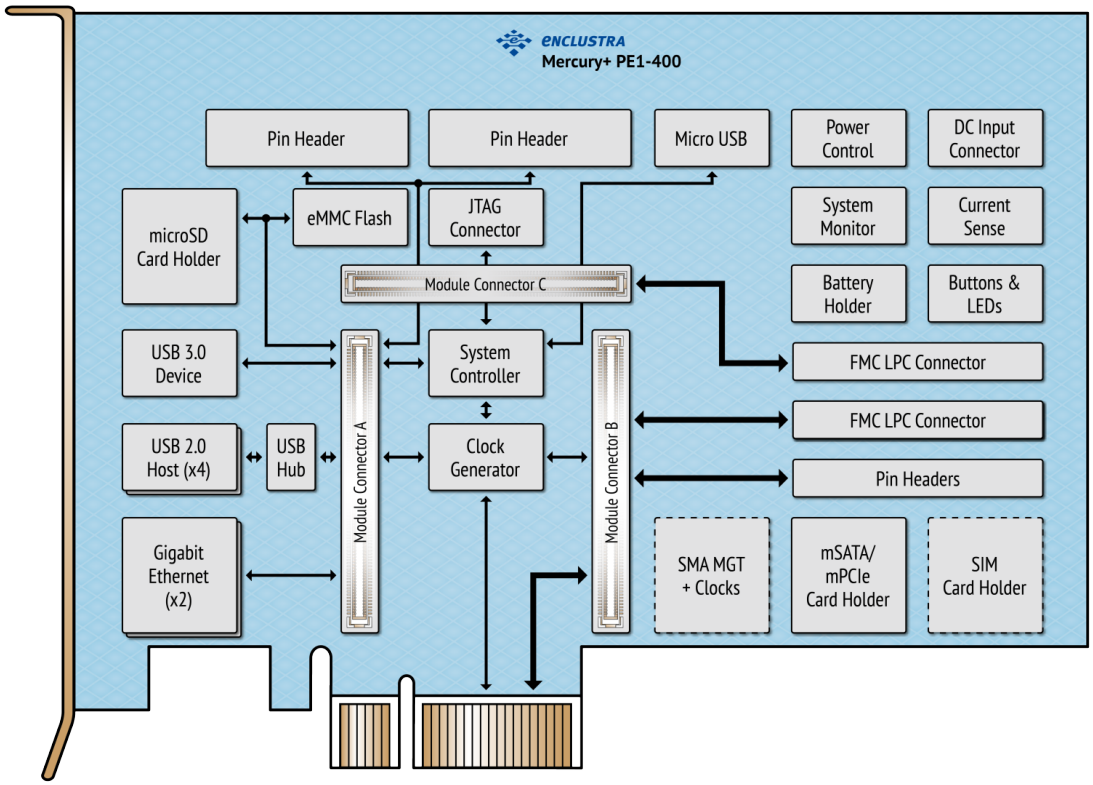

Figure 3: Hardware Block Diagram PE1-400

3.2 Features

Table 1 describes the features available on the Mercury+ PE1 base board.

Feature	Description	PE1-200	PE1-300	PE1-400
Form factor	160 × 111.15 mm × 1.6 mm (PCB only)			
Module connector	Number of 168-pin Hirose FX10 connectors	2	3	3
System features	System controller	✓	✓	✓
	Built-in Xilinx JTAG (via USB connection)	✓	✓	✓
	System monitor	✗	✓	✓
	Power control	✓	✓	✓
	Current sense	✗	✓	✓
	Low-jitter clock generator	✗	✓	✓
	Accelerometer/magnetometer/temperature sensor	✗	✓	✓
Memory	microSD card holder	✓	✓	✓
	eMMC managed NAND flash	✗	✓	✓
	User EEPROM	✓	✓	✓
Connectors	PCIe ×4 interface	✓	✓	✓
	USB 3.0 device interface	✓	✓	✓
	Number of USB 2.0 host interfaces	1	4	4
	Micro USB 2.0 device (UART, SPI, I2C, JTAG) interface	✓	✓	✓
	2 × RJ45 Gigabit Ethernet connector	✓	✓	✓
	mPCIe or mSATA card holder (in standard configuration USB only)	✗	✓	✓
	SIM card holder	✗	optional	optional
	Clock and MGT data SMA in/out connectors	✗	optional	optional
User I/Os	Number of FMC LPC connectors	1	0	2
	Number of FMC HPC connectors	0	1	0
	2 × 40-pin Anios pin headers	✓	✓	✓
	3 × 12-pin I/O connectors	✓	✓	✓
Supply voltage	12 V DC (internal, external, or PCIe)	✓	✓	✓
	USB-power (with restrictions)	✓	✓	✓

Table 1: Base Board Features and Configurations

Warning!

Please note that the available features depend on the equipped FPGA/SoC module and on the selected Mercury+ PE1 base board variant.

3.3 Board Configuration and Product Codes

Table 2 describes the standard base board configurations. Custom configurations are available; please contact Enclustra for further information.

Product Code	Features	Temperature Range
ME-PE1-200-C	Refer to Table 1	0..+70° C
ME-PE1-300-W	Refer to Table 1	-25..+85° C
ME-PE1-400-W	Refer to Table 1	-25..+85° C

Table 2: Standard Base Board Configurations

3.4 Article Numbers and Article Codes

Every board is uniquely labeled, showing the article number and serial number. An example is presented in Figure 4.

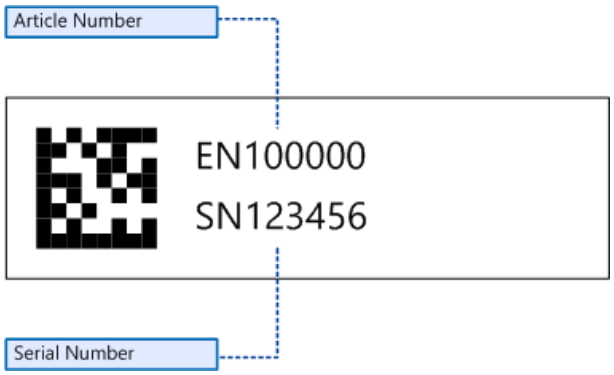

Figure 4: Product Label

The correspondence between article number and article code is shown in Table 3. The article code represents the product code, followed by the revision; the R suffix and number represent the revision number.

The revision changes and product known issues are described in the Mercury+ PE1 Base Board Known Issues and Changes document [5].

Article Number	Article Code
EN101317	ME-PE1-200-C-R4
EN101308	ME-PE1-300-W-R4
EN101309	ME-PE1-400-W-R4
EN103080	ME-PE1-200-C-R4.6
EN103081	ME-PE1-300-W-R4.6
EN103082	ME-PE1-400-W-R4.6

Table 3: Article Numbers and Article Codes

3.5 Top and Bottom Views

3.5.1 Top View

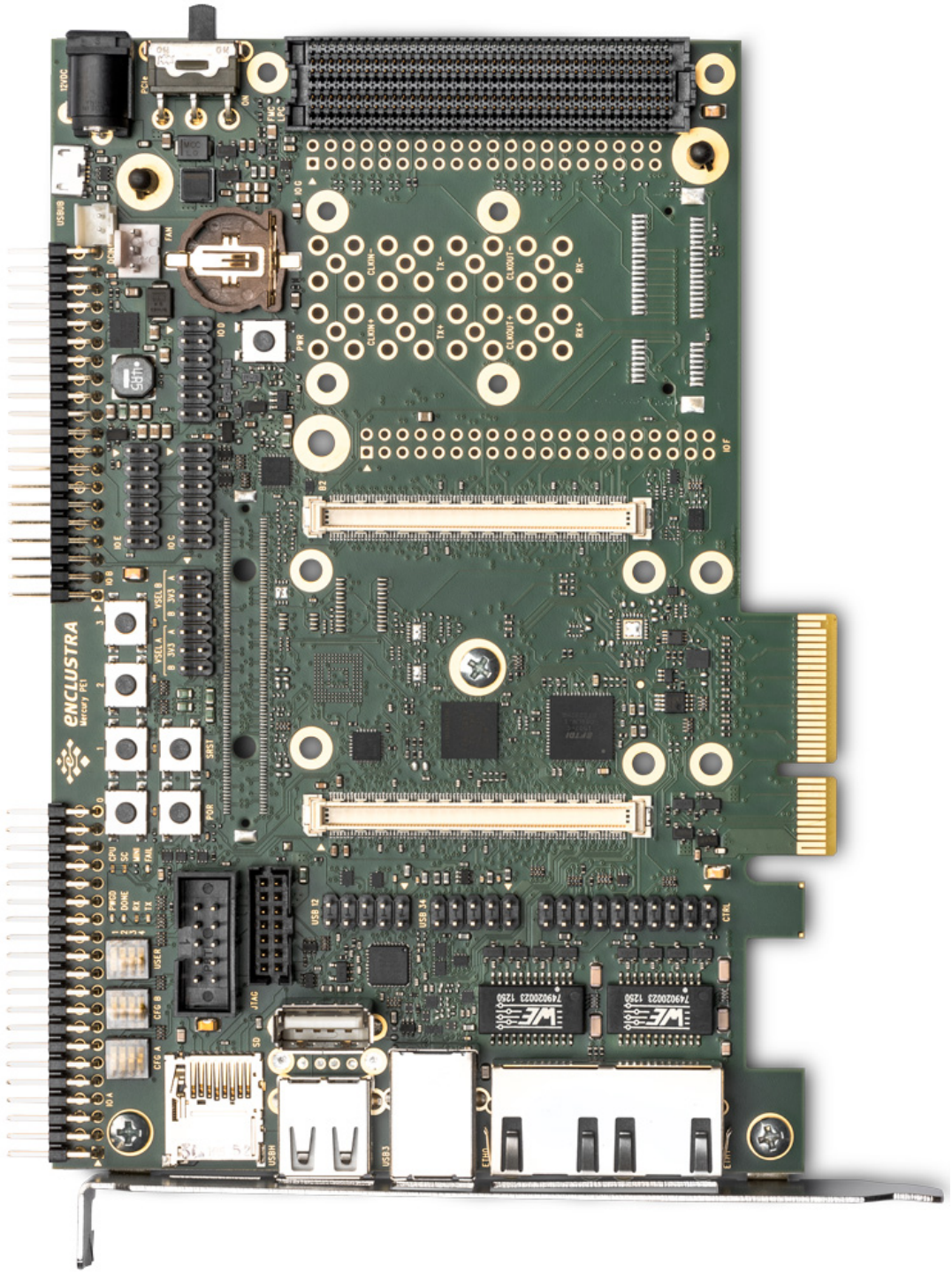

Figure 5: Board Top View PE1-200 Variant

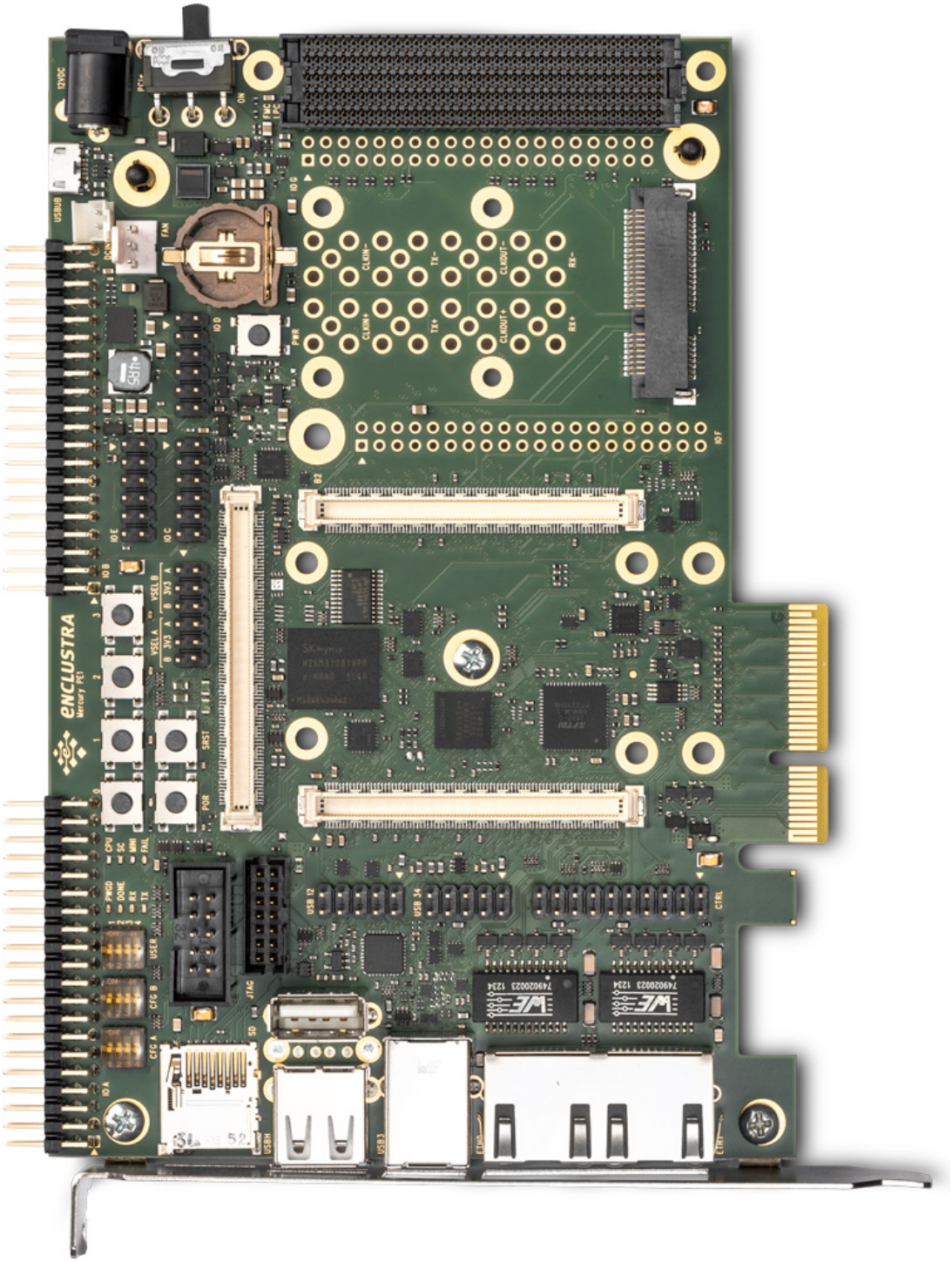

Figure 6: Board Top View PE1-300/400 Variants

3.5.2 Bottom View

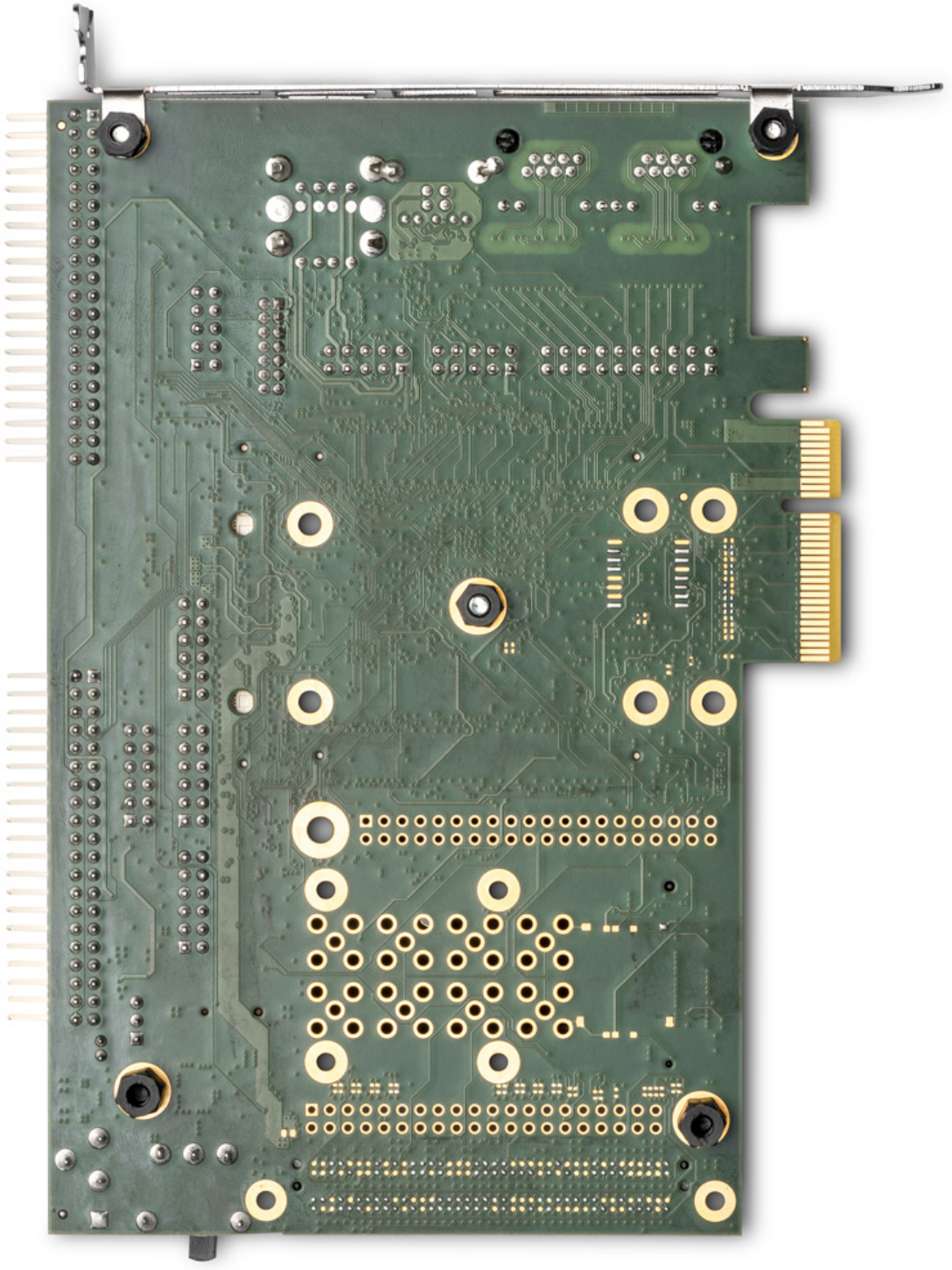

Figure 7: Board Bottom View PE1-200/300 Variants

On the PE1-400 variant, there is a second FMC LPC connector on the bottom side of the board.

Please note that depending on the hardware revision and configuration, the base board may look slightly different than shown in this document.

3.6 Top and Bottom Assembly Drawings

3.6.1 Top Assembly Drawing

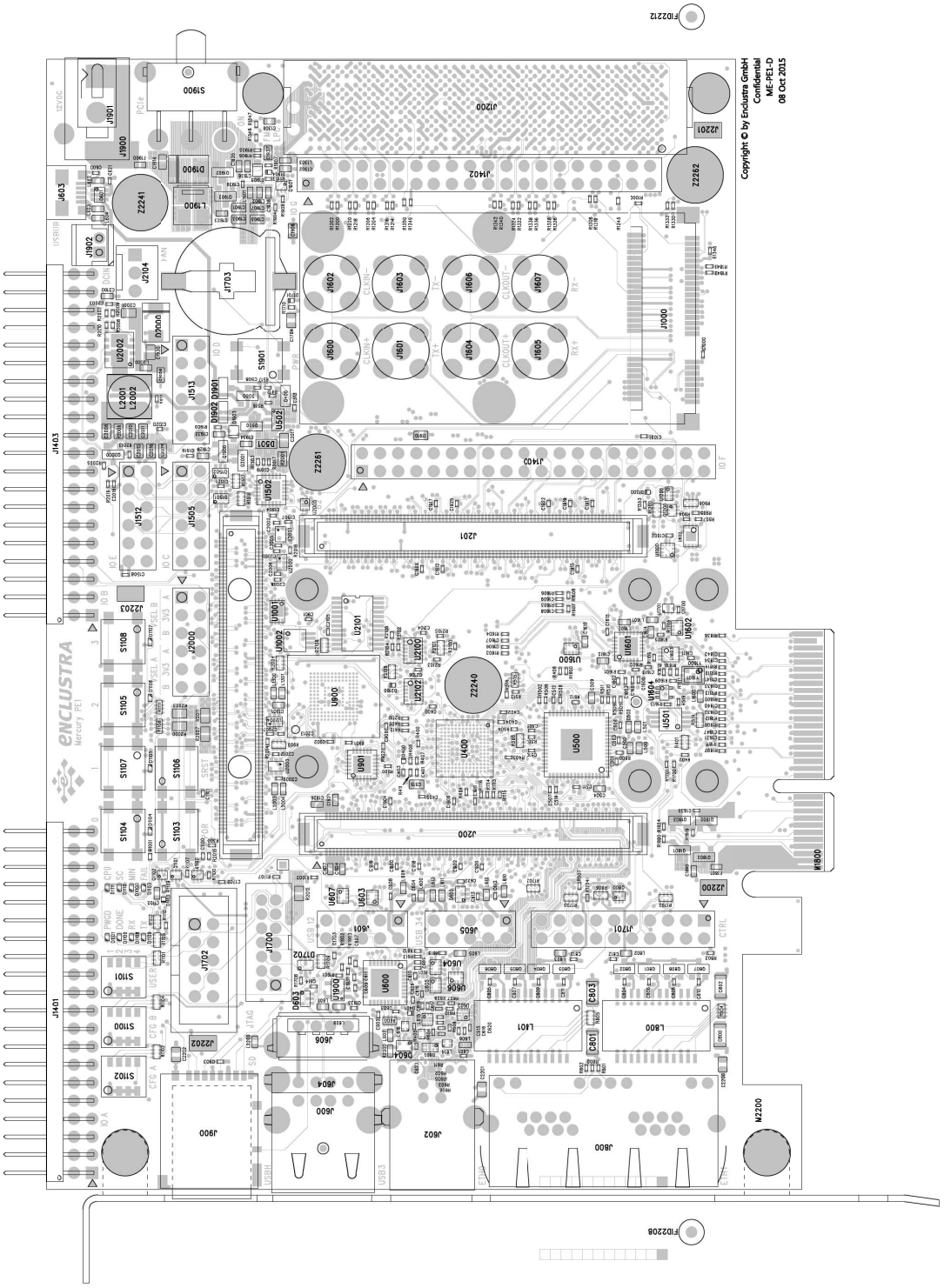

Figure 8: Board Top Assembly Drawing

3.6.2 Bottom Assembly Drawing

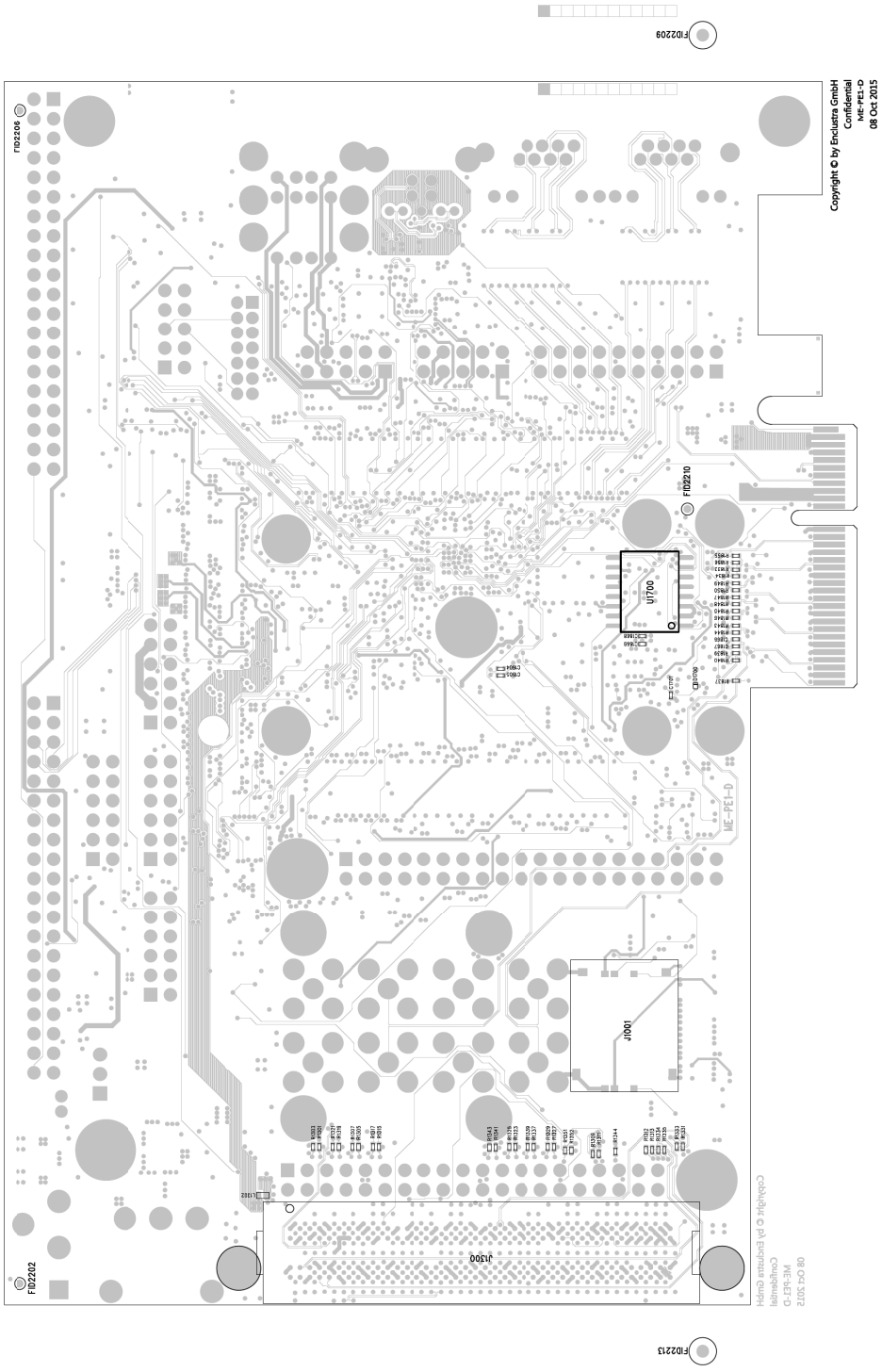

Figure 9: Board Bottom Assembly Drawing

Please note that depending on the hardware revision and configuration, the base board may look slightly different than shown in this document.

3.7 Board Dimensions

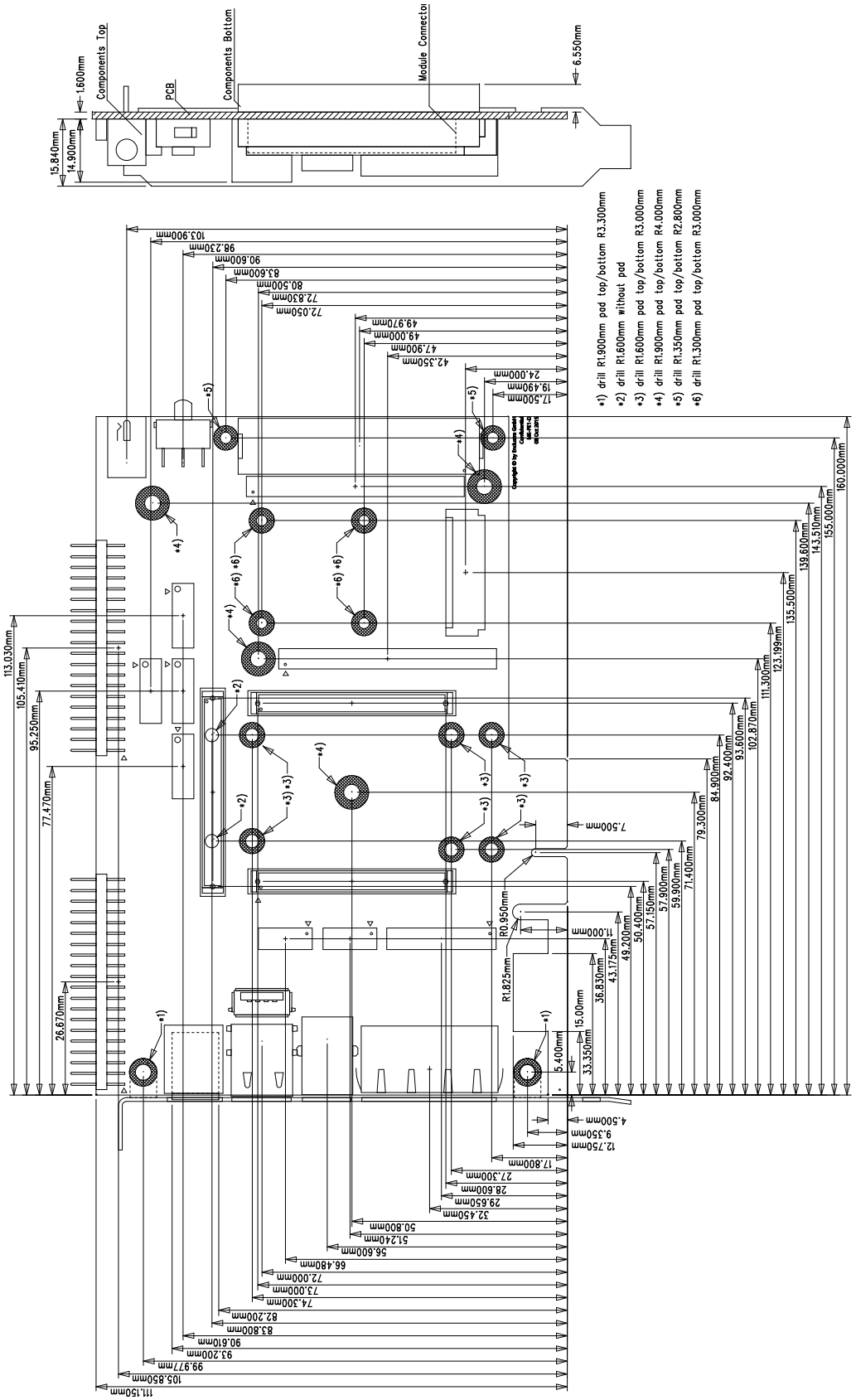

Figure 10: Board Dimensions

3.8 Bracket Drawing

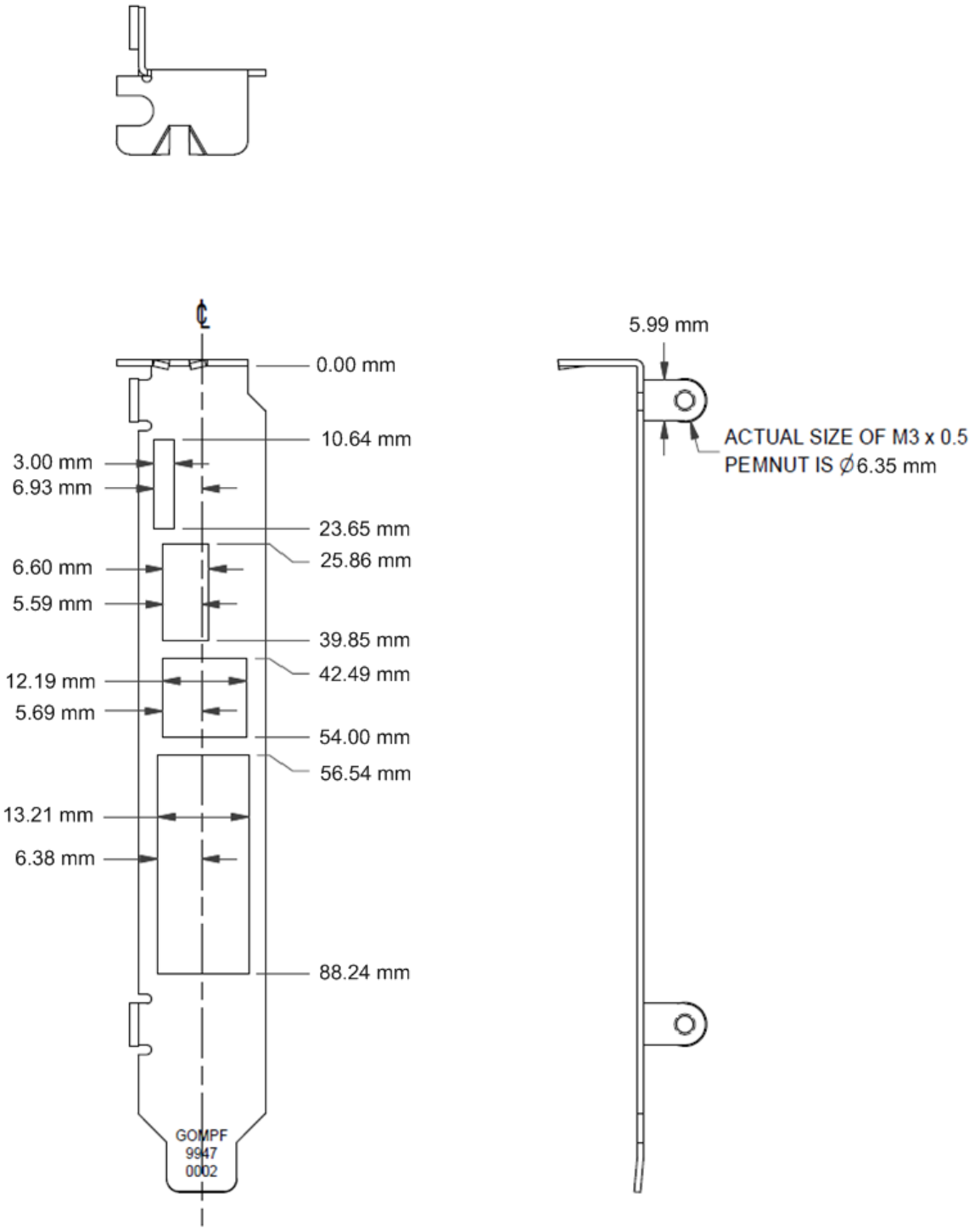

Figure 11: Bracket Drawing

3.9 Mechanical Data

Table 4 describes the mechanical characteristics of the Mercury+ PE1 base board. A 3D model (PDF) and a STEP 3D model are available [6], [7].

Symbol	Value
Size	111.15 × 160 mm (final PCB dimension, no PCIe bracket)
Component height top	16 mm
Component height bottom	6.55 mm (with PCIe bracket)
Weight	120 g (with PCIe bracket)

Table 4: Mechanical Data

3.10 Mechanical Components

Table 5 describes the mechanical components present on the Mercury+ PE1 base board. The listed elements are for reference only. Any other components that meet the requirements may be used.

Product Number	Manufacturer	Description
970060365	Würth Elektronik	2 × plastic spacer bolt with female/female thread M3, length 6 mm, bracket front
970080365	Würth Elektronik	1 × plastic spacer bolt with female/female thread M3, length 8 mm, beneath Mercury module
973080365	Würth Elektronik	3 × plastic spacer bolt with female thread/clip, length 8 mm
MPMS 003 0008 PH	B&F Fastener Supply	3 × Phillips pan head metric screws M3x8

Table 5: List of Mechanical Components

4 Connectors Description

4.1 12 V External Power (J1900)

This connector is used to supply the main VCC input voltage, when the Mercury+ PE1 base board is not powered via PCIe.

Apply only 12 V DC to this connector.

Pin Number	Signal Name	Description
1 (inner)	VCC_MAIN_IN	12 V DC (nominal) input voltage
2 (outer)	GND	Ground

Table 6: J1900 - External Power Connector

Type	Manufacturer
PJ-102AH	CUI Inc.

Table 7: J1900 - External Power Connector Type

The inner and outer diameters of the mating plug are 2.0 mm and 5.5 mm respectively.

4.2 12 V Internal Power (J1902)

The Mercury+ PE1 base board can alternatively be powered through the internal power input connector. The 12 V DC power source connected to J1902 must be filtered by external power circuitry.

Pin Number	Signal Name	Description
1	VCC_MAIN_CM	12 V DC (nominal) input voltage
2	GND	Ground

Table 8: J1902 - Internal Power Connector

Type	Manufacturer
292132-2	TE Connectivity

Table 9: J1902 - Internal Power Connector Type

Warning!
Do not short circuit the 12 V power supply, and make sure the currents flowing through the pins of the internal connector do not exceed 2.0 A. Otherwise, the PCB may be damaged. Please note that this current value may be insufficient for certain Mercury modules.

Table 10 shows an example of a mating part for the internal power connector.

Type	Manufacturer
2-179694-2	TE Connectivity

Table 10: Mating Part for the Internal Power Connector

4.3 I/O Voltage Selection (J2000)

The I/O voltage selection jumpers are used to configure the VCC_IO_A and VCC_IO_B voltages that power the I/O banks of the SoC/FPGA device on the Mercury module. Refer to Section 5.7 for details.

4.4 Mercury Module Connectors A, B, C (J200/J201/J300)

A detailed pinout of the Mercury module connectors can be found in the Mercury Master Pinout [9] and in the Mercury+ PE1 Base Board User Schematics [4].

Warning!

Only Enclustra Mercury/Mercury+ FPGA/SoC modules should be inserted into the Mercury+ PE1 base board.

Warning!

The VCC_IO pins are directly connected to the FPGA/SoC device. Apply only compliant voltages to the VCC_IO pins; any other voltage may damage the mounted Mercury FPGA/SoC module, as well as other devices on the Mercury+ PE1 base board.

4.5 USB 2.0 Host Connector (J600)

If the mounted Mercury module features a USB controller, the module's USB signals can be connected to J600 via a USB hub, allowing USB host mode operation. The power and data signals on this connector are ESD-protected.

Refer to Section 6.5 for details on USB connections.

4.6 USB 2.0 Host Connector (J606)

The USB 2.0 host connector J606 is only available for PE1-300/400 board variants.

If the mounted Mercury module features a USB controller, the module's USB signals can be connected to J606 via a USB hub, allowing USB host mode operation. The power and data signals on this connector are ESD-protected.

Refer to Section 6.5 for details on USB connections.

4.7 USB 3.0 Device Connector (J602)

Full USB 3.0 device functionality is only available with Mercury modules that have a USB 3.0 device controller.

The base board can be powered via the USB 3.0 device connector, even if the Mercury module does not support USB 3.0; further information on USB connectivity and power is available in Sections 6.5 and 5.4.

The J602 connector is protected against ESD.

4.8 Micro USB 2.0 Device Connector (J603)

The micro USB connector on the board is connected to the FTDI device via a multiplexer. It can be used for UART, SPI and I2C communication. Refer to Section 6.5 for details on USB connections.

The base board can be powered via the micro USB 2.0 device connector; further information on USB power is available in Section 5.4.

The J603 connector is protected against ESD.

4.9 USB Header Ports (J601/J605)

The USB header ports on J601 and J605 are only available for PE1-300/400 board variants. They are connected to the downstream ports of the USB 2.0 hub. The upstream port of the USB hub is routed via a multiplexer to the USB signals of Mercury module. Refer to Section 6.5 for more information on USB connections.

The power and data lines on J601 and J605 connector are protected against ESD.

4.10 Dual Gigabit Ethernet Port Eth0/Eth1 (J800-A/J800-B)

There are two 10/100/1000 Mbit Ethernet ports on the Mercury+ PE1 base board. The capabilities of the Ethernet interfaces depend on the connected Mercury module.

The RJ45 connector J800 is connected through magnetics directly to the Mercury module connector. For details on the Ethernet interface, please refer to Section 6.4.

4.11 microSD Card Slot (J900)

The enclosure of J900 is connected to GND.

The microSD card signals can be connected via a multiplexer with a built-in level shifter to the Mercury module SDIO signals. This signal path can be activated by setting the SDIO_SEL signal to logic high. This signal is controlled by the DIP switch CFG A 3 or by the system controller. Refer to Sections 6.3 and 6.16 for details on configuration.

4.12 mPCIe/mSATA Card Holder (J1000)

In the standard configuration, only the USB signals are routed to this card holder. PCIe and SATA connections are optional and require some hardware changes.

Warning!

The J1000 connector respects the mPCIe pinout standard. Note that for mSATA implementation, the receiver pairs MINI_PER0_N/P must be inverted.

4.13 SIM Smart Card Slot (J1001)

The SIM card holder is an optional component which may be assembled on PE1-300/400 board variants.

The signals on the SIM card slot are connected to the mPCIe/mSATA card holder.

4.14 FMC Connectors (J1200/J1300)

These connectors allow the extension of the Mercury+ PE1 base board with other FMC (FPGA Mezzanine Card) modules (Enclustra or third-party).

For details on the pinout of the FMC LPC (Low Pin Count) and HPC (High Pin Count), please refer to the VITA 57 FMC specification.

Table 11 describes the FMC connectors present on the Mercury+ PE1 base board, for each board variant. On the PE1-400 variant, the second FMC LPC connector is on the bottom side of the board.

Base Board Variant	Connector Pinout Type	Connector Name in the Schematics
PE1-200	FMC LPC	J1200-A, J1200-B (2 × 80-pin)
PE1-300	FMC HPC	J1200-A, J1200-B, J1200-C, J1200-D, J1200-E (5 × 80-pin)
PE1-400	FMC LPC FMC LPC	FMC LPC 0: J1200-A, J1200-B (2 × 80-pin) FMC LPC 1: J1300-A, J1300-B (2 × 80-pin)

Table 11: FMC Connectors Overview

Warning!

The FMC I/O pins are connected directly to the FPGA/SoC device. Use only VCC_IO voltages compliant with the equipped FPGA/SoC device; any other voltage may damage the mounted Mercury FPGA/SoC module, as well as other devices on the Mercury+ PE1 base board.

Board Variant	FMC Connector Name	Connector Type	Number of Connectors	Manufacturer
PE1-200	FMC LPC connector 0	ASP-134603-01	1	Samtec
PE1-300	FMC HPC connector	ASP-134486-01	1	Samtec
PE1-400	FMC LPC connector 0 FMC LPC connector 1	ASP-134603-01	2	Samtec

Table 12: J1200/J1300 - FMC HPC/LPC Connectors Type

Tables 13, 14 and 15 include information related to the total number of I/Os available on each FMC connector and assembly options.

Table 13 lists the total number of I/Os available on the LPC connector 0 and available pin types. Note that the multi-gigabit transceivers and clocks are only available in combination with modules that are equipped with a third connector (module connector C).

Signal Name	FMC Pin Type	Single Ended	Pairs	Module Connector
FMC_DP0_C2M_P/N	DP0 C2M	-	1	C
FMC_DP0_M2C_P/N	DP0 M2C	-	1	C
FMC_GCLK0_M2C_P/N	GBTCLK M2C	-	1	C
FMC_LA<...>_P/N	LA	60	30	B
FMC_LA<...>_CC_P/N	LA CC	8	4	B
FMC_CLK<...>_M2C_P/N	CLK M2C	-	2	B

Table 13: User I/Os on the FMC LPC Connector 0

Table 14 lists the number of I/Os available on the higher part of the HPC connector and available pin types. The PE1-300 board variant includes the pins listed in Tables 13 and 14. Note that the pins on the higher part of the HPC connector are only available in combination with modules that are equipped with a third connector (module connector C).

Signal Name	FMC Pin Type	Single Ended	Pairs	Assembly Option
FMC_DP<...>_C2M_P/N	DP C2M	-	3	4 additional pairs may be available; refer to Figure 12.
FMC_DP<...>_M2C_P/N	DP M2C	-	3	4 additional pairs may be available; refer to Figure 12.
FMC_HA/HB<...>_P/N	HA/HB	80	40	8 differential pairs may be disconnected from HA/HB pins and connected to DP0 C2M/M2C pins; refer to Figure 12.
FMC_HA/HB<...>_CC_P/N	HA/HB CC	12	6	-
FMC_CLK2_BIDIR_P/N	CLK BIDIR	-	2	-

Table 14: User I/Os on the Higher Part of the FMC HPC Connector

In the standard configuration, there are 4 transceiver pairs available on the HPC connector (DP0-DP3). Optionally, 8 module connector signal pairs may be disconnected from the FMC HPC HA/HB pins and connected to the FMC HPC DP transceiver pins (M2C/C2M). This connection may be useful when MGT signals from/to the FPGA or SoC device are routed on the corresponding module connector pins (C - 45, 47, 48, 50, 51, 53, 54, 56, 57, 59, 60, 62, 63, 65, 66, 68). Refer to Figure 12 for details on the FMC HPC assembly options. The standard configuration is marked in bold.

The names of the signals on the module connectors indicate to which pins of the FMC HPC connector they are routed to. For the HA/HB signals that can be rerouted to DP pairs, the naming convention is described in Figure 12.

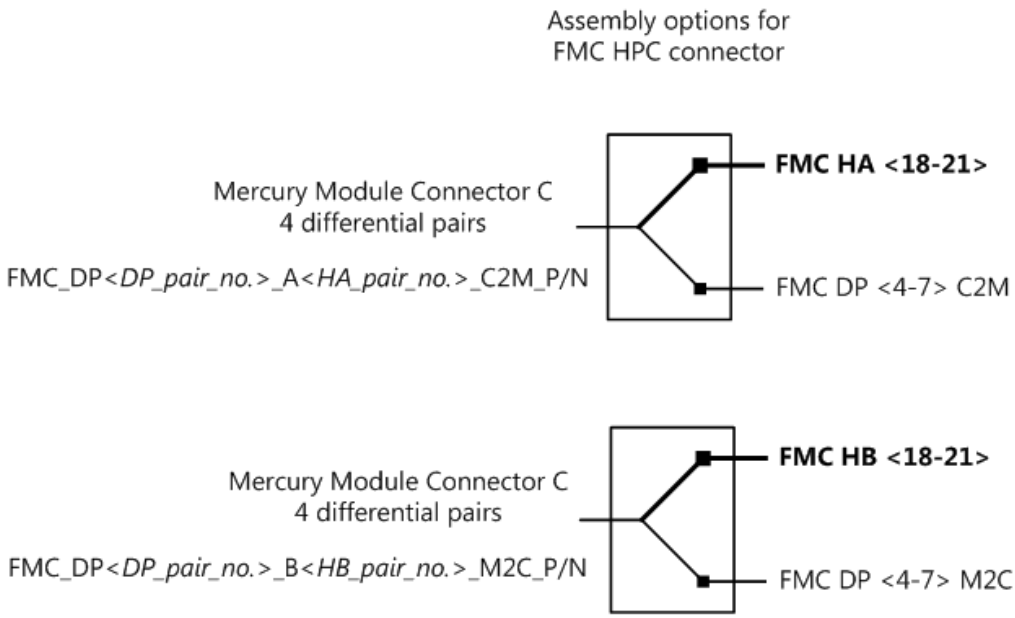

Figure 12: FMC HPC Assembly Options (only possible on PE1-300)

Table 15 lists the total number of I/Os available on the LPC connector 1 and pin types. The PE1-400 board variant includes the pins listed in Tables 13 and 15. Note that the pins on the LPC connector 1 are only available in combination with modules that are equipped with a third connector (module connector C).

One GBT clock pair may be optionally routed to a clock generator differential input (CG_CLKIN_P/N); refer to Section 6.8 for details.

Signal Name	FMC Pin Type	Single Ended	Pairs	Assembly Option
FMC1_GCLK0_M2C_P/N	GBTCLK M2C	-	1	**Hardware changes:** 1 pair can be routed to CG_CLKIN_P/N signal
FMC_HA/HB<...>_P/N	LA	60	30	-
FMC_HA/HB<...>_CC_P/N	HA/HB CC	8	4	-
FMC_CLK<...>_P/N	CLK M2C	-	2	-

Table 15: User I/Os on the FMC LPC Connector 1

4.15 Anios I/O Connectors A, B, F, G (J1401/J1403/J1400/J1402)

The Anios I/O connectors can be used for user applications: each connector provides 24 user I/Os, a differential clock connection, connectivity to the I2C bus, and power supply connections. The clock, data and I2C signals are routed to the module connector - for details, refer to the Mercury+ PE1 Base Board User Schematics [4].

Anios connectors F and G are not equipped in the standard configuration, and their signals are shared with the FMC LPC connector 0.

Warning!

The Anios I/O pins are connected directly to the FPGA/SoC device. Use only VCC_IO voltages compliant with the equipped FPGA/SoC device; any other voltage may damage the mounted Mercury FPGA/SoC module, as well as other devices on the Mercury+ PE1 base board.

Anios A Connector

- The J1401 connector is connected directly to the Mercury module connector.

Anios B Connector

- Some of the signals on J1403 connector are shared with the system controller and user buttons.

Anios F Connector

- The signals on J1400 connector are shared with the FMC LPC connector 0.

Anios G Connector

- The signals on J1402 connector are shared with the FMC LPC connector 0.

4.16 I/O Connectors C, D, E (J1505/J1513/J1512)

The 12-pin I/O connectors can be used for user applications: each connector provides 8 user I/Os and 3.3 V power supply connections.

The signals on I/O connectors C and D are routed directly to the module connector. The signals on I/O connector E are routed to the system controller and to the module connector via a multiplexer with a built-in level shifter. For details, refer to the Mercury+ PE1 Base Board User Schematics [4].

Warning!

I/O connectors C and D are routed directly to the FPGA/SoC device. Use only VCC_IO voltages compliant with the equipped FPGA/SoC device; any other voltage may damage the mounted Mercury FPGA/SoC module, as well as other devices on the Mercury+ PE1 base board.

I/O Connectors C and D

I/O connectors C and D connectors (2 × 6) are mapped directly to the Mercury module connector. These connectors are Digilent Pmod™ compatible when VCC_IO_B is 3.3V.

Warning!

Do not insert a PMOD module to these connectors if VCC_IO_B is not 3.3 V, as this may damage the mounted Mercury FPGA/SoC module, as well as other devices on the Mercury+ PE1 base board.

I/O Connector E

Half of the signals on I/O Connector E are connected to the module connector and on-board LEDs via a multiplexer with a built-in level shifter. Figure 13 shows the signals connections; the default connection is marked in bold.

The rest of the signals are connected to the system controller.

This connector is Digilent Pmod™ compatible, because the I/O voltage of some of the pins is shifted to 3.3 V and the other pins are configured to a 3.3 V I/O standard in the system controller.

All I/Os connected to I/O connector E have 100 Ω series resistors.

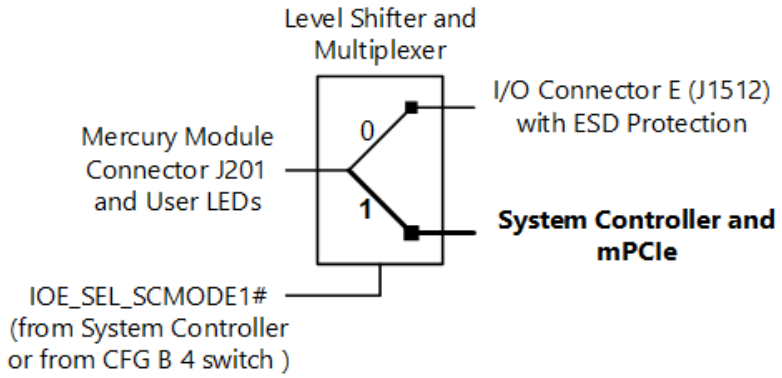

Figure 13: Overview of I/O Connector E Connections

The level shifter connection in the data path of the I/O connector E is controlled by the signal IOE_SEL_SCMODE1#. This signal can be modified by setting the configuration DIP switches or the system controller registers. Please refer to Section 6.3 and 6.16 for details.

IOE_SEL_SCMODE1#	Effect
0	The signals from the module connector are routed to I/O connector E
1	The signals from the module connector are routed to the mPCIe card holder and to the system controller

Table 16: IOE_SEL_SCMODE1# Signal Usage

4.17 Clock Input SMA Connectors (J1600/J1602)

These connectors are optional components which may be assembled on PE1-300/400 board variants. If they are equipped, the signals can be connected to the clock generator circuit via some multiplexers. Refer to Sections 6.8 and 6.16 for details on clock path configuration. By default, the connection from the SMA connectors to the clock generator is not active.

Further information on the clock SMA connectors is available in the Mercury+ PE1 Base Board User Schematics [4].

Connector Number	Connector Pin	Signal Name	Description
J1600	1	CLKIN_P	Positive clock input
	SHIELD	GND	Ground
J1602	1	CLKIN_N	Negative clock input
	SHIELD	GND	Ground

Table 17: J1600/J1602 - Clock Input SMA Connectors Connections

Table 18 shows the type of the SMA connector; the same type is used for all SMA connectors on the Mercury+ PE1 base board (if they are equipped).

Type	Manufacturer
142-0701-201	Johnson / Cinch Connectivity Solutions

Table 18: SMA Connector Type

4.18 Clock Output SMA Connectors (J1604/J1606)

These connectors are optional components which may be assembled on PE1-300/400 board variants. If they are equipped, the signals can be connected to the clock generator circuit via some multiplexers. Refer to Sections 6.8 and 6.16 for details on clock path configuration. By default, the connection from the clock generator to the SMA connectors is not active.

Further information on the clock SMA connectors is available in the Mercury+ PE1 Base Board User Schematics [4].

Connector Number	Connector Pin	Signal Name	Description
J1604	1	CLKOUT_P	Positive clock output
	SHIELD	GND	Ground
J1606	1	CLKOUT_N	Negative clock output
	SHIELD	GND	Ground

Table 19: J1604/J1606 - Clock Output SMA Connectors Connections

4.19 Data Input SMA Connectors (J1605/J1607)

These connectors are optional components which may be assembled on PE1-300/400 board variants. If they are equipped, the signals can be connected to the FPGA MGT receiver pairs. One of the 4 MGT RX pairs connected to the PCIe edge connector can be rerouted to the SMA data input connectors; this requires some electronic components to be removed, while others need to be soldered on the board.

Further information on the data SMA connectors is available in the Mercury+ PE1 Base Board User Schematics [4].

Connector Number	Connector Pin	Signal Name	Description
J1605	1	SMA_RX_P	Positive data receive
	SHIELD	GND	Ground
J1607	1	SMA_RX_N	Negative data receive
	SHIELD	GND	Ground

Table 20: J1605/J1607 - Data Input SMA Connectors Connections

4.20 Data Output SMA Connectors (J1601/J1603)

These connectors are optional components which may be assembled on PE1-300/400 board variants. If they are equipped, the signals can be connected to the FPGA MGT transmitter pairs. One of the 4 MGT TX pairs connected to the PCIe edge connector can be rerouted to the SMA data input connectors; this requires some electronic components to be removed, while others need to be soldered on the board.

Further information on the data SMA connectors is available in the Mercury+ PE1 Base Board User Schematics [4].

Connector Number	Connector Pin	Signal Name	Description
J1601	1	SMA_TX_P	Positive data transmit
	SHIELD	GND	Ground
J1603	1	SMA_TX_N	Negative data transmit
	SHIELD	GND	Ground

Table 21: J1601/J1603 - Data Output SMA Connectors Connections

4.21 Battery Holder (J1703)

A 3 V lithium battery (CR1220) can be installed for buffering the real-time clock on the connected Mercury FPGA/SoC module. The battery is not included.

Alternatively, the VCC_BAT_IN power signal can be driven via pin 6 of connector J1701. Refer to Section 4.23 for details.

Warning!

There is a danger of explosion if the battery is replaced incorrectly - only replace the battery with the same or equivalent type recommended by Enclustra.

Used batteries should be disposed of according to the manufacturer's instructions.

4.22 FPGA JTAG Connectors (J1700/J1702)

The FPGA JTAG connectors allow access to the JTAG port of the mounted Mercury FPGA/SoC module. The signals on these connectors are protected against ESD. Series termination resistors are equipped between the module signals and the JTAG headers.

The standard JTAG connectors available on the Mercury+ PE1 base board can be used in combination with Xilinx Platform Cable USB or Altera USB-Blaster download cable.

JTAG_PRESENT# signal is used to determine if an external JTAG adapter is connected; the external adapter should tie this signal to GND when the cable is plugged in.

Xilinx JTAG Connector

Pin Number	Pin Name	Connection
1, 3, 5, 7, 9, 11	GND	Ground
2	VCC	VCC_IO_A
4	TMS	JTAG_TMS
6	TCK	JTAG_TCK
8	TDO	JTAG_TDO
10	TDI	JTAG_TDI
12	NC	Not connected
13	GND	JTAG_PRESENT#
14	NC	SRST#_RDY

Table 22: J1700 - Xilinx JTAG Connector

Altera JTAG Connector

Pin Number	Pin Name	Connection
1	TCK	JTAG_TCK
2	GND	JTAG_PRESENT#
3	TDO	JTAG_TDO
4	VCC	VCC_IO_A
5	TMS	JTAG_TMS
6	NC	SRST#_RDY
7, 8	NC	Not connected
9	TDI	JTAG_TDI
10	GND	Ground

Table 23: J1702 - Altera JTAG Connector

Warning!

The JTAG pins are connected to the FPGA/SoC device via small series resistors. Use only VCC_IO voltages compliant with the equipped FPGA/SoC device. Any other voltages may damage the equipped FPGA/SoC device as well as other devices on the module or Mercury+ PE1 base board.

4.22.1 Xilinx JTAG over System Controller

The system controller includes built-in Xilinx JTAG programmer functionality, making it possible to use a USB connection for JTAG debugging. It is fully supported by the Xilinx tools.

The following steps need to be taken in order to use the Xilinx JTAG:

- Set the FTDI device in Xilinx JTAG mode using the Enclustra Module Configuration Tool (MCT) [10]
- Set the ScMode0 register to 0 (refer to Sections 6.3 and 6.16)
- Set the USB_SEL signal so that the currently used USB connector is routed to the FTDI device (refer to Sections 6.3 and 6.5)

4.22.2 Altera JTAG over System Controller

Currently, the built-in Altera JTAG functionality is not supported by the system controller.

4.23 Control Connector (J1701)

The control connector is used mainly for control and monitoring purposes. Many different control functions are affected by the signals connected to this connector. Detailed information can be found in Table 24.

Pin Number	Signal Name	Description	Function
1	VCC_MAIN_CM	12 V DC main voltage	Supply output/ Monitor
2	GND	Ground	-
3	VCC_5V	5 V DC-DC converter output	Supply output/ Monitor
4	VCC_3V3_SC	3.3 V DC voltage for the system controller power	Monitor
5	UART_RX_EXT	External connection UART RX, configurable via system controller registers See Section 6.16 for details	Control
6	VCC_BAT_IN	External connection for battery supply	Supply input/ Monitor
7	UART_TX_EXT	External connection UART TX, configurable via system controller registers See Section 6.16 for details	Control
8	PWR_GOOD	Power good status	Monitor
9	PWR_BTN#	External connection for power button	Control
10	PWR_EN	Power enable status	Control
11	GND	Ground	-
12	FTDI_BDBUS7_SCJTAGEN	Reserved for internal use	-
13	SYSMON_GPI	General purpose input to the system monitor	Control
14	FTDI_BDBUS0_SCTCK_TXD	Reserved for internal use	-
15	SYSMON_GPO#	General purpose output from the system monitor	Monitor
16	FTDI_BDBUS1_SCTDI_RXD	Reserved for internal use	-
17	POR#_LOAD#	External connection for power-on reset signal	Control
18	FTDI_BDBUS2_SCTDO	Reserved for internal use	-
19	FPGA_DONE	FPGA configuration done status	Monitor
20	FTDI_BDBUS3_SCTMS	Reserved for internal use	-

Table 24: J1701 - Control Connector

4.24 PCIe ×4 Edge Connector (M1800)

The Mercury+ PE1 base board has a PCIe ×4 edge connector, which allows to use the board with standard CPU motherboards which have a PCIe slot. The edge connector complies with the PCIe standard - the PCIe pinout is documented in the PCIe specification available on the PCI SIG website.

Note that for the PE1-300/400 board variants, the PCIe reference clock is routed via the clock generator to the MGT reference clock. On start-up the PCIe clock is forwarded to the MGT clock pair; this setup is done by the system controller. Details are available in Sections 6.8 and 6.16.

On the PE1-200 variant, the PCIe reference clock is routed directly to the MGT reference clock, by using some bypass capacitors.

4.25 Fan Connector (J2104)

An external 12 V fan with a sense signal can be connected to J2104 connector.

Pin Number	Signal Name	Description
1	GND	Ground
2	VCC_MAIN	12 V DC main voltage
3	SYSMON_TACHO	Sense signal to determine fan speed. Refer to Section 6.9 for details.

Table 25: J2104 - Fan Connector Connections

5 Power

5.1 Power Input

The Mercury+ PE1 base board can be powered using one of the power input sources listed below:

- External power connection through J1900 connector
- Internal power connection through J1902 connector
- PCIe power connection
- USB VBUS power connection

The standalone configuration of the Mercury+ PE1 base board requires external/internal power connections or USB power connection. In this case the board is not used as a PCIe card.

5.2 Power Slide Switch

Table 26 describes the power slide switch behavior; the factory default is marked in bold.

Slide Connection	Slide Position	Effect
1-2	**Towards external power connector (position marked with "PCIe" inscription)**	The board is powered via the PCIe edge connector M1800 or via USB
3-2	Towards FMC connector (position marked with "ON" inscription)	The board is powered through the external connector (J1900) or internal connector (J1902) or via USB

Table 26: S1900 - Power Slide Switch

5.3 Power over PCIe

By default, the Mercury+ PE1 base board is powered over PCIe via the edge connector. Power source selection is performed by setting the power slide switch (see Table 26).

Warning!

It is possible to power the PCIe power supply pins by the on-board power supply. Drive EIO_12V_EN# and EIO_3V3_EN# signal low to obtain PCIe power output - note that this does not correspond to the PCIe specification. Refer to Section 6.7 for more information.

When using power over PCIe, make sure that the power over USB is disabled; please refer to Section 5.4 for details.

5.4 Power over USB

As soon as a USB cable is plugged into the Mercury+ PE1 base board, the system controller and the FTDI USB 2.0 device controller are powered over USB; this will cause the SC LED to blink.

If external USB power is enabled, the Mercury+ PE1 base board and the mounted Mercury module are powered over USB. In this case, VCC_MAIN is connected to the USB input voltage. Table 27 describes the VBUS power control; the factory default is marked in bold.

DIP Switch CFG A 2	USB_PWR_EN#	Effect
OFF	**1**	**USB power is not connected to the VCC_MAIN domain. An external supply must be connected to the board.**
ON	0	USB power (5 V) is connected to VCC_MAIN domain. The Mercury+ PE1 base board is powered via the USB connector (J602 or J603).

Table 27: USB - VBUS Control

Warning!

If the Mercury module is powered via USB, make sure that it does not consume more power than the USB specification allows.

5.5 Power Control

Power control is enabled and disabled by the PWR_ON# signal, determined by the position of the DIP switch CFG A 4. Table 28 describes the power control configuration; the factory default is marked in bold.

DIP Switch CFG A 4	PWR_ON#	Effect
OFF	**1**	**Power control is ON**
{ON	0	Power control is OFF

Table 28: Power Control Switch Configuration

If power control is disabled, the Mercury+ PE1 base board and the mounted module are powered as soon as power is applied through external or internal power connectors and the power slide switch is set accordingly.

If power control is enabled, the Mercury module is not powered, even when power is applied to the Mercury+ PE1 base board. By pressing the power button (PWR) for a short time, the power is turned on. Power can be turned off again by pressing the power button for a configurable time. Power can also be turned on and off by writing a system controller register - see Section 6.16 for more information.

Power control is not available when power over USB is active.

5.6 Power Sequencing

The on-board VCC_3V3 power domain is switched on when all the power supplies on the module and board are within their range (PWR_GOOD signal is high).

PWR_GOOD	Effect
0	VCC_3V3 domain is switched off
1	VCC_3V3 domain is switched on

Table 29: Power Sequencing

5.7 I/O Voltage Selection

The I/O voltage selection jumpers are used to configure the VCC_IO_A and VCC_IO_B voltages that power the I/O banks of the SoC/FPGA device on the Mercury module.

Tables 30 and 31 describe the usage of jumpers. Please note the following:

- VCC_OUT_A and VCC_OUT_B voltages are supply outputs from the Mercury module. The value of the voltages depends on the mounted Mercury module (Refer to the "Voltage Supply Outputs" Section in the Mercury module user manual).
- Only one jumper per VCC_IO_A, respectively VCC_IO_B is allowed (one choice per table)
- The factory default jumper settings are 2-4 and 8-10. As a consequence of these settings, no voltage is applied to the Mercury module connector, therefore it prevents the module from booting. PWGD LED will not be lit.

Figure 14 shows the pin numbering for connector J2000 and one configuration example.

Jumper	Position	Function	Description
J2000	7-8	VCC_OUT_A selected	Module VCC_OUT_A is connected to VCC_IO_A
J2000	9-10	VCC_3V3 selected	VCC_3V3 is connected to VCC_IO_A
J2000	11-12	VCC_OUT_B selected	Module VCC_OUT_B is connected to VCC_IO_A

Table 30: Jumper Settings VCC_IO_A

Jumper	Position	Function	Description
J2000	1-2	VCC_OUT_A selected	Module VCC_OUT_A is connected to VCC_IO_B
J2000	3-4	VCC_3V3 selected	VCC_3V3 is connected to VCC_IO_B
J2000	5-6	VCC_OUT_B selected	Module VCC_OUT_B is connected to VCC_IO_B

Table 31: Jumper Settings VCC_IO_B

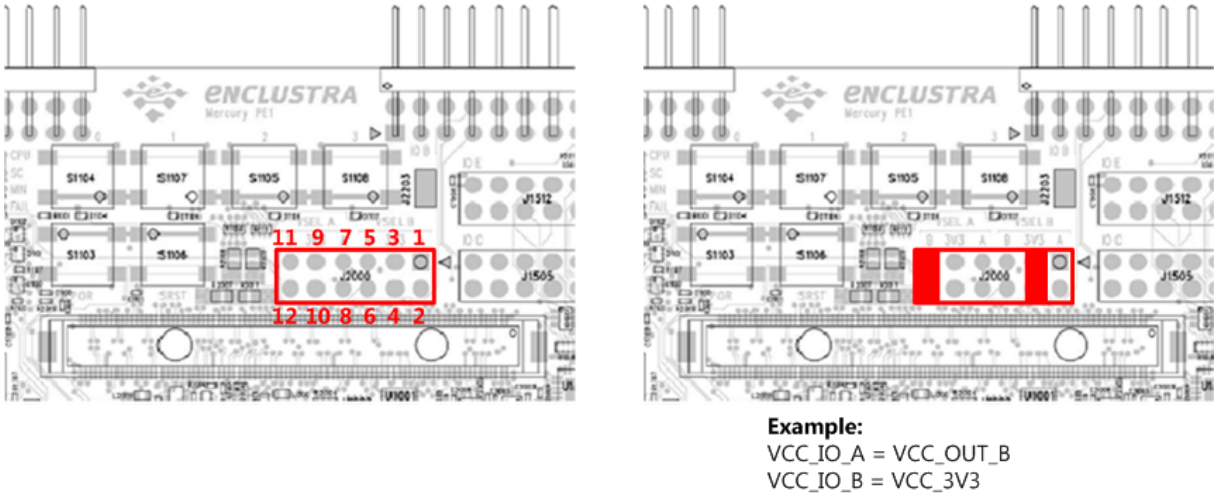

Figure 14: VCC_IO Jumper Positions - Pin Numbering and Configuration Example

6 Board Function

6.1 LEDs

Table 32 describes the function of the LEDs on the Mercury+ PE1 base board.

LED Name	LED	Signal Name	Controlled by	Description
PWGD	D1101	PWR_OK#	Power circuits	Indicates that PWR_GOOD is active and VCC_IO_A and VCC_IO_B are available
DONE	D1100	FPGA_DONE	Mercury module	FPGA configuration is done
RX	D1108	NOR_MISO_RXLED#	System controller	UART RX status, shared with SPI NOR flash MISO signal
TX	D1109	NOR_MOSI_TXLED#	System controller	UART TX status, shared with SPI NOR flash MOSI signal
CPU	D1111	NOR_CLK_CPULED#	System controller	CPU status, shared with SPI NOR flash CLK signal
SC	D1110	NOR_CS#_SCLED#	System controller	System controller status, shared with SPI NOR flash CS signal
MINI	D1000	MINI_LED#	mPCIe card	mPCIe card activity status
FAIL	D1103	-	Power circuits	Indicates that one of the power supplies is failing or the voltage configuration is incorrect
0	D1104	IOE_D0_LED0#	Module connector or I/O connector E Refer to Section 4.16.	User LED 0
1	D1105	IOE_D1_LED1#		User LED 1
2	D1106	IOE_D2_LED2#		User LED 2
3	D1107	IOE_D3_LED3#		User LED 3

Table 32: Board LEDs

The user I/O LEDs can have various functions on the Mercury+ PE1 base board.

For details on the LED connections, refer to Sections 4.16 and 6.16 and to the Mercury+ PE1 Base Board User Schematics [4].

Figure 15 presents the location of the LEDs and buttons on the Mercury+ PE1 base board. This represents a snapshot from the assembly drawing in which the LEDs are marked with red, and the buttons are marked with blue.

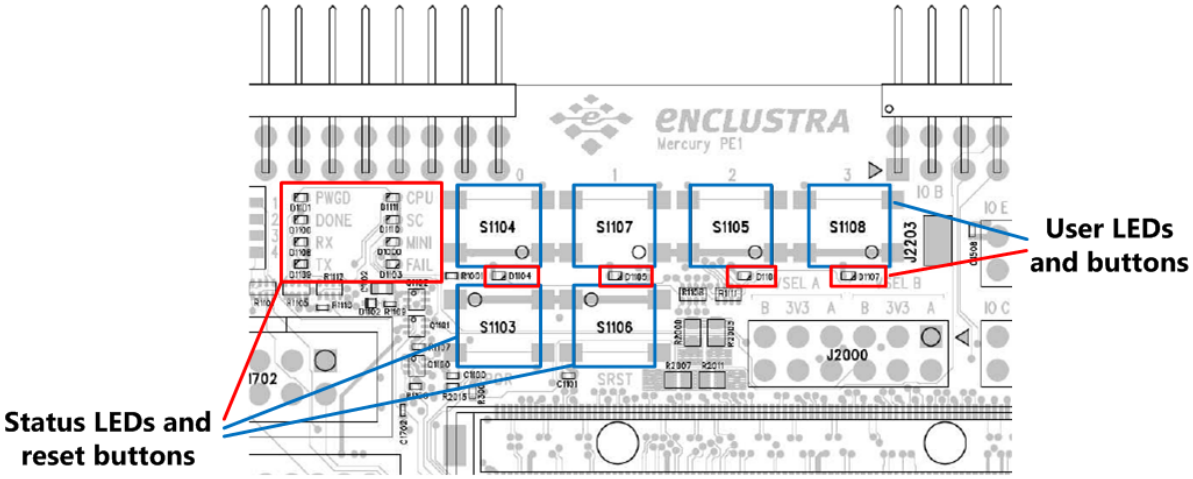

Figure 15: LEDs and Buttons - Assembly Drawing Top View

6.2 Buttons

All buttons are active-low; their function is described in Table 33. The user buttons can be configured by the user to have various functions. For details, refer to Section 6.16 and to the Mercury+ PE1 Base Board User Schematics [4].

Button Name	Button	Signal Name	Function	Comments
PWR	S1901	PWR_BTN#	Power on/off	Refer to Section 5.5
POR	S1103	POR#_LOAD#	Power-on reset/ Configuration-clear	Refer to the Enclustra Module Pin Connection Guidelines [8]
SRST	S1106	SRST#_RDY#	Soft-reset/ Configuration-delay	Refer to the Enclustra Module Pin Connection Guidelines [8]
0	S1104	IOB_D20_SC4_BTN0#	User function	Shared with the system controller, module connector and Anios I/O connector B
1	S1107	IOB_D21_SC5_BTN1#	User function	Shared with the system controller, module connector and Anios I/O connector B
2	S1105	IOB_D22_SC6_BTN2#	User function	Shared with the system controller, module connector and Anios I/O connector B
3	S1108	IOB_D23_SC7_BTN3#	User function	Shared with the system controller, module connector and Anios I/O connector B

Table 33: Board Buttons

6.3 DIP Switches

There are three configuration switches on the Mercury+ PE1 base board: CFG A, CFG B and USER; the latter one can be configured by the user to have various functions.

Tables 34 and 35 describe the function of the CFG A and CFG B switches; the factory default is marked in bold.

Warning!

Please note that the DIP switches must be configured according to the connectivity requirements. The factory default configuration does not implicitly indicate a valid configuration. The DIP switches may require different settings depending on the equipped module.

For details on the board configuration, refer to Section 6.16 and to the Mercury+ PE1 Base Board User Schematics [4].

DIP Switch	Signal Name	Pos.	Effect	Comments
CFG A 1	BOOT_MODE0	**OFF**	**BOOT_MODE0 is set to 1**	Refer to the Mercury module user manual
		ON	BOOT_MODE0 is set to 0	
CFG A 2	USB_PWR_EN#	**OFF**	**Power over USB OFF**	Refer to Section 5.4
		ON	Power over USB ON	
CFG A 3	SDIO_SEL	**OFF**	**SD card active**	SDIO_SEL is set to 1: the SDIO signals from module connector are routed to the SD card
		ON	eMMC flash active	SDIO_SEL is set to 0: the SDIO signals from module connector are routed to the eMMC flash
CFG A 4	PWR_ON#	**OFF**	**Power control ON**	Refer to Section 5.5
		ON	Power control OFF	

Table 34: S1102 - Configuration Switch A

DIP Switch	Signal Name	Pos.	Effect	Comments
CFG B 1	USB_ID	**OFF**	**The module USB signals are routed to the USB 3.0 device connector**	Refer to Section 6.5
		ON	The module USB signals are routed to the USB hub upstream	
CFG B 2	USB_SEL	**OFF**	**On startup: BOOT_MODE1 is set to 1**	Refer to Section 6.5
			After startup: The FTDI signals are routed to the micro USB connector	
		ON	On startup: BOOT_MODE1 is set to 0	
			After startup: The FTDI signals are routed to the USB 3.0 device connector	
CFG B 3	VMON_SEL_SCMODE0#	**OFF**	**On startup: ScMode0 register is set to 1**	Refer to Sections 6.16 and 6.9
			After startup: VMON_SEL is set to 1	
		ON	On startup: ScMode0 register is set to 0	
			After startup: VMON_SEL is set to 0	
CFG B 4	IOE_SEL_SCMODE1#	**OFF**	**On startup: UsbMode register is set to 1**	Refer to Sections 6.16 and 4.16
			After startup: IOE_SEL_SCMODE1# is set to 1	
		ON	On startup: UsbMode register is set to 0	
			After startup: IOE_SEL_SCMODE1# is set to 0	

Table 35: S1100 - Configuration Switch B

Warning!

The switch configuration CFG B 1 OFF and CFG B 2 ON is not permitted, and may damage the Mercury+ PE1 base board and equipped Mercury module.

Some of the configuration switches have different functions, on startup and after startup; these switches are connected to the system controller, which reads the switch positions on startup and defines the behavior of certain circuit elements accordingly.

When powering the system controller, the switch has the "On startup" effect; afterwards the switch can be toggled to obtain the required hardware configuration.

Note that the system controller is powered when either a USB cable is attached, or when the main power is applied. For example, if the application requires that BOOT_MODE1 is set to 1 and that the FTDI signal is routed to the USB 3.0 connector, the user should follow these steps:

- Switch off the power supply of the board
- Disconnect all USB cables from the board
- Configure the DIP switches for the desired boot mode
- Plug the USB cable into the USB 3.0 connector (in order to power up the system controller, so that the "On startup" switch setting is latched)
- Configure the DIP switches for the FTDI path routing
- Power up the board using 12 V DC

Please refer to Section 6.16 for details on system controller inputs that are read at startup.

Tables 36 and 37 describe the meaning of the ScMode0 and UsbMode registers and their influence on the Mercury+ PE1 base board functionality. Details on these registers can be found in Section 6.16.

ScMode0 Register	Effect
0	The system controller has Xilinx JTAG functionality
1	The system controller has Altera JTAG functionality (currently not supported)

Table 36: ScMode0 Register Usage

UsbMode Register	Effect	Description
0	USB_MODE is set to 0	Module connector pins A131 and A133 are connected to USB_ID signal and to the VBUS pins of the USB 2.0 header ports[1]
1	USB_MODE is set to 1	Module connector pins A131 and A133 are connected to the upstream port (DP/DN pins) of the USB 2.0 hub[1]

Table 37: UsbMode Register Usage

Warning!

The switch configuration CFG B 1 ON (activate connection from module USB DP/DN signals to USB 2.0 hub) and CFG B 4 OFF (activate connection from module USB ID/VBUS signals to USB 2.0 hub) is not permitted, and may damage the Mercury+ PE1 base board and equipped Mercury module.

The ScMode0 and UsbMode registers of the system controller can also be configured using I2C. Refer to Section 6.16 for details.

[1]USB_MODE set to 1 is required for Mercury modules that are equipped with a second USB PHY. In this case, pins A127 and A129 are connected to the first USB PHY data signals, while pins A131 and A133 are connected to the second USB PHY data signals. Refer to section 6.5 for details on USB connections.

The user switches can be configured by the user to have various functions. For details, refer to Section 6.16 and to the Mercury+ PE1 Base Board User Schematics [4].

DIP Switch	Signal Name	Function	Connection
USER 1	IOB_D16_SC0_DIP1#	User defined	Module connector, system controller, user buttons, Anios I/O connector B
USER 2	IOB_D17_SC1_DIP2#	User defined	Module connector, system controller, user buttons, Anios I/O connector B
USER 3	IOB_D18_SC2_DIP3#	User defined	Module connector, system controller, user buttons, Anios I/O connector B
USER 4	IOB_D19_SC3_DIP4#	User defined	Module connector, system controller, user buttons, Anios I/O connector B

Table 38: S1101 - User Configuration Switch

6.4 Ethernet

The Mercury+ PE1 base board is equipped with a dual Gigabit Ethernet port, configured according to the capabilities of the mounted module.

The Ethernet magnetics and the RJ45 connectors are equipped on the base board, while the Ethernet PHY is equipped on the Mercury module.

Each of the two RJ45 connectors can be used as 1 Gigabit Ethernet port or as 2 × 10/100 Mbit Ethernet ports, depending on the equipped Mercury module.

If one of the RJ45 connectors on the board is used for a dual Fast Ethernet implementation, an external RJ45 Y-adapter/splitter is required in order to convert the 4-pairs connection into 2 × 2-pairs connections.

6.5 USB

6.5.1 USB Overview

Figure 16 presents an overview of the USB connections on the Mercury+ PE1 base board. The default configuration is marked in bold.

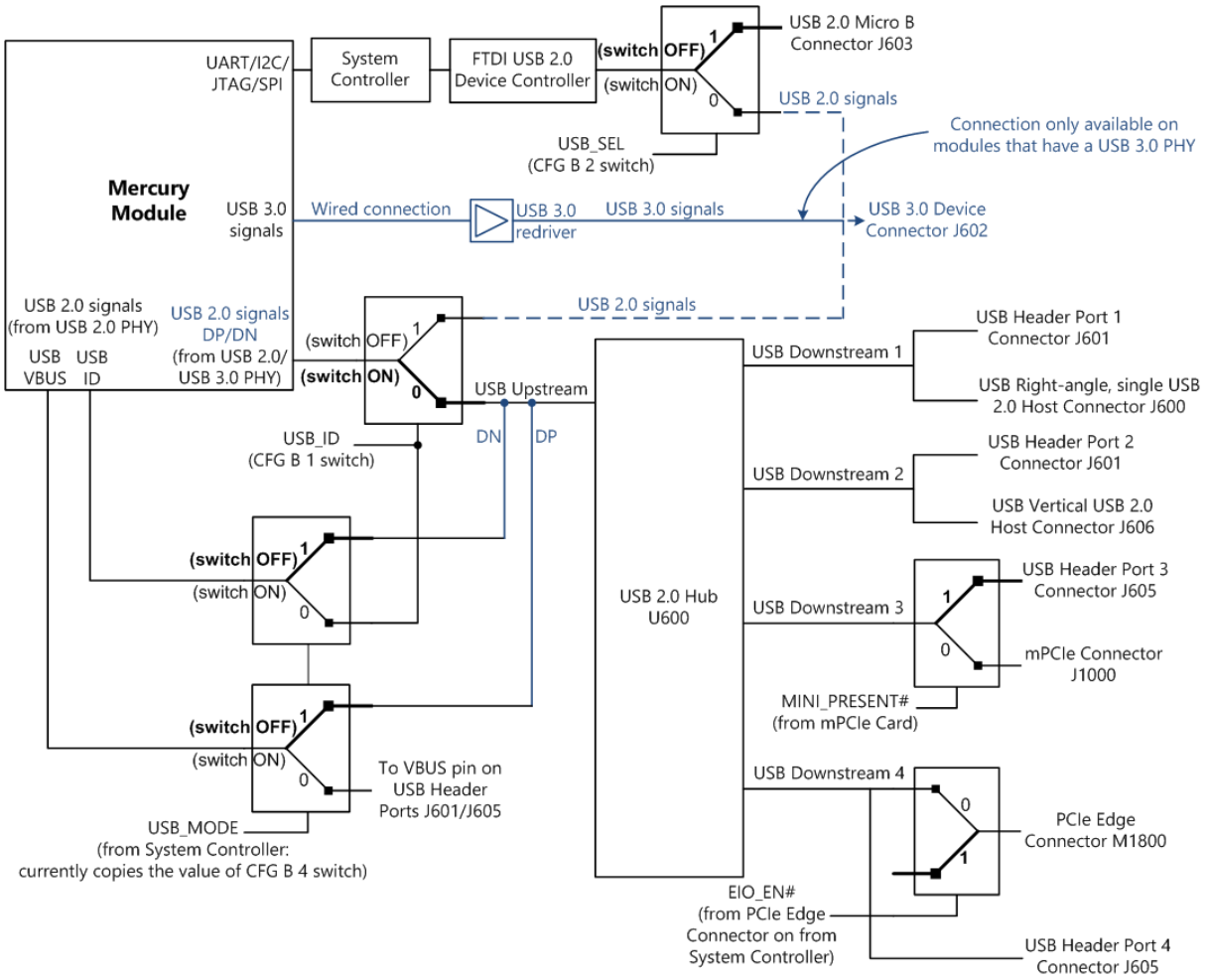

Figure 16: USB Connections Overview

Full USB 3.0 device functionality is only available with Mercury modules that have a USB 3.0 device controller. The connection for the USB 3.0 (SuperSpeed) signals on the J602 device connector is hard-wired. The connection for the USB 2.0 DP/DN signals on the J602 device connector can be selected via two multiplexers: the signals can be either connected to the FTDI device, or to the USB 2.0 PHY/USB 3.0 PHY present on the module.

The FTDI device can be connected either to the USB 2.0 micro B connector, or to the USB 3.0 device connector (without USB 3.0 functionality). The FTDI connection can be used for configuration or test purposes.

Warning!

The switch configuration CFG B 1 OFF (activate connection from module USB DP/DN signals to USB 3.0 device connector) and CFG B 2 ON (activate connection from FTDI to USB 3.0 device connector) is not permitted, and may damage the Mercury+ PE1 base board and equipped Mercury module.

Some Mercury modules have a second USB port connected to the USB ID and VBUS signals on the module connector (pins A131 and A133). The second USB port can be routed to the USB 2.0 hub by setting USB_MODE signal to high; this can be done by configuring DIP switch CFG B 4 to OFF - refer to Section 6.3 for details on board configuration.

Warning!

The switch configuration CFG B 1 ON (activate connection from module USB DP/DN signals to USB 2.0 hub) and CFG B 4 OFF (activate connection from module USB ID/VBUS signals to USB 2.0 hub) is not permitted, and may damage the Mercury+ PE1 base board and equipped Mercury module.

6.5.2 USB 2.0 Device Controller (FTDI)

The FTDI FT2232HQ USB 2.0 device controller present on the Mercury+ PE1 base board can be used to easily implement a communication link to a host PC.

The FTDI device is connected to the system controller and can be used for various communication protocols. Details on the FTDI modes and configuration can be found in Section 6.16.

By default, the UART communication between the FTDI device and FPGA is active. The Xilinx JTAG mode can be activated using the Enclustra MCT [10] and is independent of the UART connection.

The library used by the MCT is available free of charge; it allows users to integrate module enumeration, FPGA and SPI flash configuration, and I2C communication functionality in their own application. The library consists of a Windows DLL with a C-style interface, allowing use of the library from almost any programming language; for C++ applications, a C++ wrapper is also provided. Please contact Enclustra for details.

6.6 I2C Communication

There are several I2C devices on the Mercury+ PE1 base board, connected to the I2C communication lines. These are presented in Table 39.

Note that the I2C signals connected to the Mercury connector address other I2C devices equipped on the Mercury module.

Board Reference	Function	I2C Address (7-bit)	Comments
J200	Mercury module	-	Additional devices are available on the Mercury module
U400	System controller	0x0D	
U2101	System monitor	0x2F	
U1601	Clock generator	0x70	
U902	User EEPROM	0x57	
U1000	Accelerometer Magnetometer	0x1D 0x1E	
J1401	Anios I/O connector A	User-defined	
J1403	Anios I/O connector B	User-defined	
J1400	Anios I/O connector F	User-defined	
J1402	Anios I/O connector G	User-defined	

Table 39: I2C Bus System

The following devices can be addressed using I2C if they have been previously activated by the signal I2C_EN_FMC. This signal can be toggled by setting a system controller register. Refer to Section 6.16 for details.

BoardReference	Function	I2C Address
J1200-B	FMC HPC/LPC connector 0	User-defined
J1300-B	FMC LPC connector 1	User-defined
J1000	mPCIe	User-defined

Table 40: I2C_EN_FMC Controlled Functions

The following device can be addressed using I2C if this feature has been previously activated in the system controller (currently not supported). Refer to Section 6.16 for details.

Board Reference	Function	I2C Address
M1800	PCIe ×4 edge connector	User-defined

Table 41: System Controller Controlled Functions

6.7 PCIe

The PCIe ×4 edge connector can be used in two hardware configurations:

1. PCIe endpoint standard configuration - ×1, ×2 or ×4 PCIe communication between the equipped Mercury module and a PCIe host/motherboard. In this configuration:
   - The FPGA acts as a PCIe endpoint
   - It complies with the PCIe standard
   - The Mercury+ PE1 base board is powered over PCIe (see Section 5.3)
   - Only on PE1-300/400 board variants: the clock generator must be configured to enable the PCIe reference clock - by default, the configuration of the clock generator is done by the system controller at power-up (see Section 6.8).
2. PCIe non-standard configuration - usage of the Mercury+ PE1 base board as standalone board, and connection to a custom board via the PCIe ×4 edge connector. In this configuration:
   - The FPGA acts as a PCIe host (note that this is not a standard PCIe root complex configuration)
   - The Mercury+ PE1 base board provides a power supply connection to the custom board. The EIO_12V_EN# (PCIe edge connector, pin B3) signal must be driven low from the custom board.
   - The Mercury+ PE1 base board provides a clock and a USB connection to the custom board. The EIO_3V3_EN# (PCIe edge connector, pin B8) signal must be driven low from the custom board.

     This setting will enable the EIO_EN# signal. This signal will, in turn, activate a connection to a downstream port of the USB hub, and a clock output; both connections are on the JTAG pins of the PCIe edge connector. Refer to Table 42 and Sections 6.5 and 6.8 for details. The default configuration is marked in bold.

     Note that EIO_EN# signal value can be overwritten from the system controller registers. Refer to Section 6.16 for details.

   In this configuration, the FPGA operates as a PCIe host by providing an output clock connection and power supply outputs. Special hardware (custom PCIe backplane) is required to connect the Mercury+ PE1 base board to other PCIe endpoints, as this is not a standard root complex configuration.

EIO_EN#	USB Connection	Clock Generator Connection
0	USB hub downstream port 4 is connected to EIO USB	Clock generator output CG_CLKOUT_P/N is connected to PCIe edge connector
1	**EIO USB is open**	**Clock generator output CG_CLKOUT_P/N is connected to clock SMA output connectors**

Table 42: EIO Enable Signal Description

6.8 Clock Generator

The Mercury+ PE1 base board features a clock generator circuit addressable and configurable via I2C. The circuit is only available on PE1-300/400 board variants.

On the PE1-200 board variant capacitors have been mounted to forward the PCIe reference clock connection to the MGT reference clock (bypass the clock generator).

Type	Manufacturer
Si5338B-B-GMR	Silicon Labs

Table 43: Clock Generator Type

The clock generator is configured at power-up by the system controller via I2C. By default, the PCIe reference clock available on the differential input IN1/IN2 of the clock generator circuit is copied to the MGT reference clock pair 0 (MGT_REFCLK0_P/N).

The Si5338B device can be reconfigured to desired functionality via the I2C interface. Silicon Labs provides a tool that allows the user to specify several settings, such as the input clock pins and clock frequency, the output clock frequencies and phase shifts. These settings can be exported and used in the software code to configure the clock generator.

For details on features and configuration, refer to the Si5338B datasheet.

The clock generator may be loaded with default values from its non-volatile memory (NVM) at power-up, which is a one-time programmable (OTP) memory. Configuring the NVM OTP memory of the clock generator equipped on the Mercury+ PE1 base board voids the board warranty.

Warning!
Writing the contents of the NVM OTP configuration memory voids the board warranty.

6.8.1 Overview

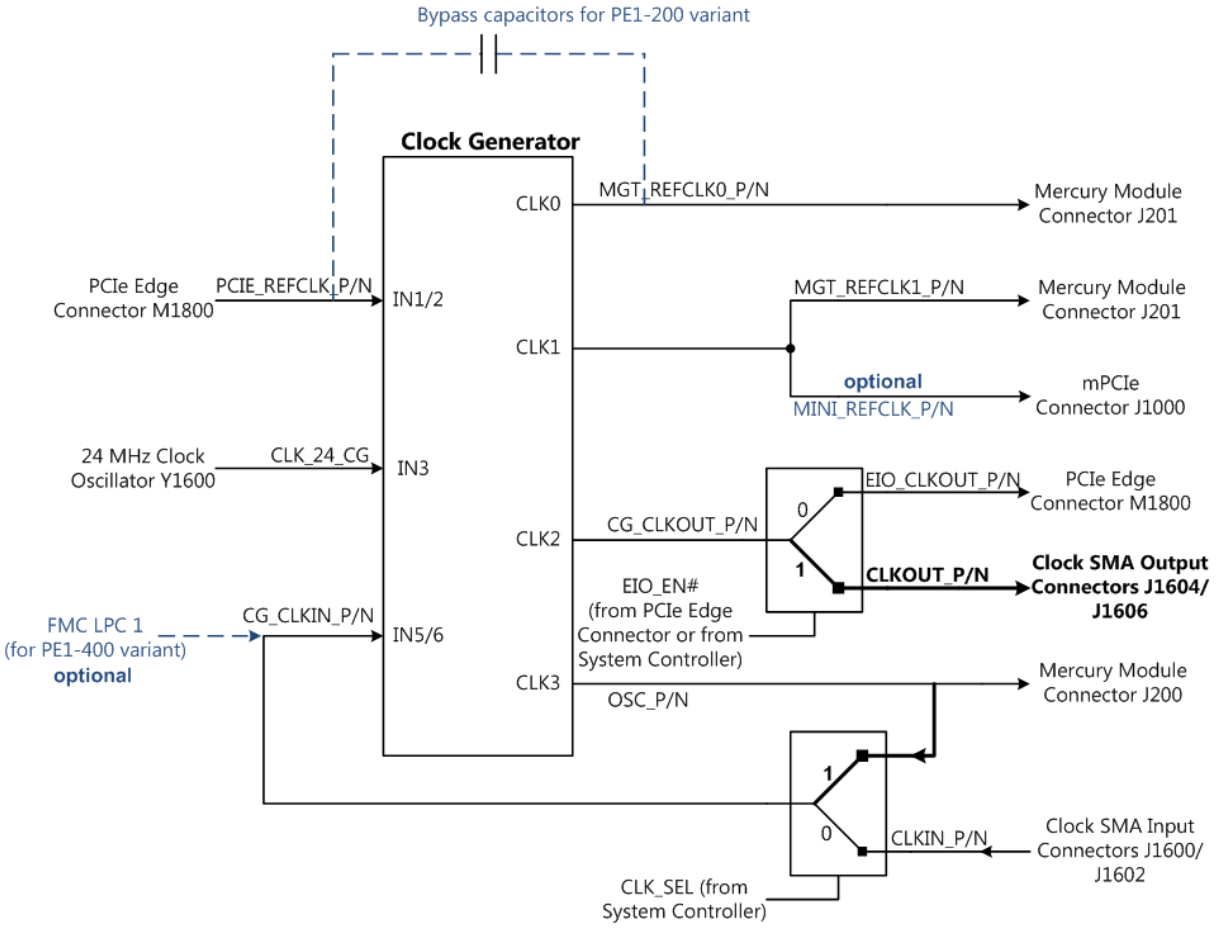

Figure 17: Clock Generator Overview

The connections to the clock generator are configurable via clock multiplexers and various circuit elements that can be mounted/removed in order to enable/disable different clock paths. For details, please refer to the Mercury+ PE1 Base Board User Schematics [4].

6.8.2 Signal Description

Clock Generator Pin	Signal Name	Connection
IN1	PCIE_REFCLK_P	PCIe edge connector M1800
IN2	PCIE_REFCLK_N	PCIe edge connector M1800
IN3	CLK_24_CG	24 MHz clock oscillator Y1600
IN5	CG_CLKIN_P	Clock SMA input connector J1600 or clock generator output CLK3A (selectable with CLK_SEL signal) or from FMC LPC connector 1 (with hardware changes, only possible on PE1-400)

Continued on next page...

Clock Generator Pin	Signal Name	Connection
IN6	CG_CLKIN_N	Clock SMA input connector J1602 or clock generator output CLK3B (selectable with CLK_SEL signal) or from FMC LPC connector 1 (with hardware changes, only possible on PE1-400)
CLK0A	MGT_REFCLK0_P	Mercury connector J201
CLK0B	MGT_REFCLK0_N	Mercury connector J201
CLK1A	MGT_REFCLK1_P	Mercury connector J201
	MINI_REFCLK_P (optional)	mPCIe connector J1000 (with hardware changes)
CLK1B	MGT_REFCLK1_N	Mercury connector J201
	MINI_REFCLK_N (optional)	mPCIe connector J1000 (with hardware changes)
CLK2A	EIO_CLKOUT_P or CLKOUT_P	PCIe edge connector M1800 or clock SMA output connector J1604 (selectable with EIO_EN#)
CLK2B	EIO_CLKOUT_N or CLKOUT_N	PCIe edge connector M1800 or clock SMA output connector J1606 (selectable with EIO_EN#)
CLK3A	OSC_P	Mercury connector J200 and clock generator input IN5 (when CLK_SEL signal is high)
CLK3B	OSC_N	Mercury connector J200 and clock generator input IN6 (when CLK_SEL signal is high)

Table 44: Clock Generator Connections

Table 45 describes the configuration settings for the clock multiplexers connected to the clock generator circuit. The default configuration is marked in bold.

Signal Name	Value	Comments
CLK_SEL	0	CG_CLKIN pins are driven by the clock SMA input connectors J1600/J1602
	1	**CG_CLKIN pins are driven by the clock generator circuit**
EIO_EN#	0	CG_CLKOUT pins drive PCIe edge connector M1800 pins
	1	**CG_CLKOUT pins drive the clock SMA output connectors J1604/J1606**

Table 45: Clock Multiplexers Control

6.9 System Monitor/Current Sense

The Mercury+ PE1 base board features a system monitor and current sense circuit, addressable via I2C - these are used for voltage and current monitoring. Additional functionality, such as GPIO and fan control, is also available.

The circuit is only available on PE1-300/400 board variants.

Type	Manufacturer
LM96080	Texas Instruments

Table 46: System Monitor Type

The system monitor performs two sets of voltage and current measurements. The user can select which set of inputs should be measured by toggling the value of the VMON_SEL signal. This can be set via the DIP switches, or via the system controller registers. Please refer to Sections 6.3 and 6.16 for details.

Board Reference	Signal Name	System Monitor Register	VMON_SEL	Comments
-	VMON_12V	IN0	0	5 - 12 V
-	VMON_3V3	IN1	0	3.3 V ±5%
-	VMON_OUT_A	IN2	0	VCC_OUT_A ±5% (module dependent)
-	VMON_OUT_B	IN3	0	VCC_OUT_B ±5% (module dependent)
-	VMON_CS_MOD	IN4	0	VCC_MAIN current
-	VMON_CS_3V3	IN5	0	VCC_3V3_MOD current
-	VMON_5V	IN6	0	5 V ±10%
J200.102	VMON_A102	IN0	1	Module dependent
J201.8	VMON_B8	IN1	1	Module dependent
J201.167	VMON_B167	IN2	1	Module dependent
J201.168	VMON_B168	IN3	1	Module dependent
-	VMON_CS_A	IN4	1	VCC_IO_A current
-	VMON_CS_B	IN5	1	VCC_IO_B current
-	VREF_CS	IN6	1	VREF current sensor

Table 47: System Monitor Voltage Connections

Board Reference	Signal Name	System Monitor Register	Description
J2104.3	SYSMON_TACHO	FAN1	Fan speed sense signal
J1701.13	SYSMON_GPI	GPI(CI)	General purpose input
J1701.15	SYSMON_GPO#	GPO#	General purpose output

Table 48: System Monitor I/O and Fan Connections

6.10 eMMC Managed NAND Flash

The eMMC flash is only assembled on PE1-300/400 board variants.

The eMMC managed NAND flash signals can be connected via a multiplexer with a built-in level shifter to the Mercury module SDIO signals. This signal path can be activated by setting the SDIO_SEL signal to logic low. This signal is controlled by the DIP switch CFG A 3 or by the system controller. Refer to Sections 6.3 and 6.16 for details on configuration.

6.11 User EEPROM

The Mercury+ PE1 base board features a user EEPROM which may be accessed via I2C. It can be used to store user data (e.g. a serial number) and can be accessed by the FPGA and by the system controller.

Type	Manufacturer
24AA128T-I/MNY	Microchip

Table 49: User EEPROM Type

6.12 SPI NOR Flash

The SPI NOR flash is not equipped in the standard configuration of the Mercury+ PE1 base board. The current system controller firmware does not support communication between the SPI NOR flash and the Mercury module.

6.13 Accelerometer/Magnetometer/Temperature Sensor

The Mercury+ PE1 base board features an accelerometer/magnetometer/temperature sensor chip accessible via I2C. This is only available for PE1-300/400 board variants.

For details on the circuit, please refer to the product datasheet.

Type	Manufacturer
LSM303CTR	ST Microelectronics

Table 50: Accelerator/Magnetometer/Temperature Sensor Type

Starting with revision 4.6 boards the accelerometer/magnetometer/temperature sensor chip is not equipped any longer. Please refer to the Mercury+ PE1 Base Board Known Issues and Changes [5] document for details.

6.14 mPCIe/mSATA Card Holder

The mPCIe/mSATA card holder is only equipped on PE1-300/400 board variants.

In the standard configuration, only the USB signals are routed to the card holder. These signals are activated by the presence of a mPCIe card that automatically drives MINI_PRESENT# signal low. Refer to Section 6.5 for details on the USB connection to the mPCIe card.

PCIe and SATA connections are configurable via various circuit elements that can be mounted/removed in order to enable/disable different clock and data paths. Please refer to the Mercury+ PE1 Base Board User Schematics [4] for details on mPCIe/mSATA connections.

Please check the pinout for the mPCIe in the design software tools (Vivado, Quartus) corresponding to the FPGA/SoC device equipped on the module used in combination with the Mercury+ PE1 base board. It is recommended to do this check by instantiating all IP cores that use MGT lines, in order to make sure that there are enough resources for the implementation, and that the lanes are correctly placed.

Warning!

Please note that Intel devices do not support PCIe lane swapping and require PCIe lane 0 to be mapped to a specific transceiver location, which does not correspond to the transceiver pair that can be routed to the mPCIe card holder on the Mercury+ PE1 base board. Enclustra Intel modules do not support mPCIe in combination with the Mercury+ PE1 base board.

Warning!

For most Enclustra Xilinx Zynq Ultrascale+ modules the mPCIe/mSATA lane on the Mercury+ PE1 base board corresponds to a GTR transceiver (except for ME-XU5 G1 configurations).

Please note that the Xilinx Zynq Ultrascale+ devices require PCIe lane 0 to be placed on GTR lane 0, which does not correspond to the transceiver pair that can be routed to the mPCIe card holder on the Mercury+ PE1 base board. Therefore Enclustra Xilinx Zynq Ultrascale+ modules (except for ME-XU5 G1 variants) do not support mPCIe in combination with the Mercury+ PE1 base board.

Signal Name	Connection
MINI_WAKE#	System controller and optionally
MINI_PERST#	Mercury module connector and LEDs
MINI_CLKREQ#	(selectable with IOE_SCMODE1# signal).
MINI_WDISABLE#	Refer to Figure 13.

Table 51: mPCIe/mSATA Interface

6.15 SIM Smart Card Slot

The SIM card holder is an optional component which may be assembled on PE1-300/400 board variants. It can be accessed by the mPCIe card.

6.16 System Controller

The Mercury+ PE1 base board is equipped with a Lattice CPLD, LCMXO2-4000HC, with the role of a system controller managing the default function of the board and providing additional functions required to operate various interfaces.

Table 52 describes the system controller firmware versions programmed on the Mercury+ PE1 base board. The listed zip archives are available on the Enclustra download page.

Revision	System Controller Firmware Version	Documentation and Upgrade Instructions
R1-R4	Mercury_PE1-R4_System_Controller_Upgrade.zip	Included in the .zip archive and in the old Mercury PE1 User Manual (R1-R3)
R4.6 and newer	Mercury_PE1-R4-6_System_Controller_Upgrade.zip	Included in the .zip archive

Table 52: System Controller Firmware Versions

Please refer to the Mercury+ PE1 Base Board Known Issues and Changes [5] document for details on the system controller firmware update on revision R4.6.

Contact Enclustra support for further information.

7 Operating Conditions

7.1 Absolute Maximum Ratings

Table 53 indicates the absolute maximum ratings for Mercury+ PE1 base board.

Symbol	Description	Rating	Unit
VCC_MAIN_IN	Supply voltage relative to GND	-0.5 to 16	V
VCC_IO_[x]	VCC I/O input voltage relative to GND	Refer to the Mercury module user manual	
$T_{ambient}$	Ambient temperature range for commercial boards (C) *	0 to +70	°C
	Ambient temperature range for wide range boards (W) *	-25 to +85	°C
T_{stor}	Storage temperature	-25 to +85	°C

Table 53: Absolute Maximum Ratings

7.2 Recommended Operating Conditions

Table 54 indicates the recommended operating conditions for Mercury+ PE1 base board.

Symbol	Description	Rating	Unit
VCC_MAIN_IN	Supply voltage relative to GND	5 to 12	V
VCC_IO_[x]	VCC I/O input voltage relative to GND	Refer to the Mercury module user manual	
$T_{ambient}$	Ambient temperature range for commercial boards (C) *	0 to +70	°C
	Ambient temperature range for wide range boards (W) *	-25 to +85	°C
T_{stor}	Storage temperature	-25 to +85	°C

Table 54: Recommended Operating Conditions

Warning!

** The components used on the hardware are specified for the relevant temperature range. The user must provide adequate cooling in order to keep the temperature of the components within the specified range.*

8 Ordering and Support

8.1 Ordering

Please use the Enclustra online request/order form for ordering or requesting information:
`http://www.enclustra.com/en/order/`

8.2 Support

Please follow the instructions on the Enclustra online support site:
`http://www.enclustra.com/en/support/`

List of Figures

List of Tables

References

[1] Enclustra General Business Conditions
http://www.enclustra.com/en/products/gbc/
[2] Enclustra FPGA Manager IP Solution
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