Mars EB1 Base Board

User Manual

Purpose

The purpose of this document is to present the characteristics of Mars EB1 base board to the user, and to provide the user with a comprehensive guide to understanding and using the Mars EB1 base board.

Summary

This document first gives an overview of the Mars EB1 base board followed by a detailed description of its features and configuration options. In addition, references to other useful documents are included.

Product Information	Code	Name
Product	MA-EB1	Mars EB1 Base Board

Document Information	Reference	Version	Date
Reference / Version / Date	D-0000-307-001	06	22.07.2021

Approval Information	Name	Position	Date
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Document History

Version	Date	Author	Comment
06	22.07.2021	DIUN	Added information on R2.5 boards and system controller firmware
05	16.02.2021	DIUN	Cleaned-up product variants, added information on module connector type, other style updates
04	08.01.2019	DIUN	Removed information on I2C connectivity on HDMI connector
03	05.05.2017	DIUN	Minor corrections and clarifications, updated dimensions
02	27.12.2016	DIUN	Minor style updates
01	24.03.2016	DIUN	Version 01 (without system controller)

Table of Contents

1 Overview

1.1 General

1.1.1 Introduction

The Mars EB1 base board is equipped with a multitude of I/O connectors for use with Mars family FPGA and SoC modules. The board is well-suited for rapid prototyping and for building FPGA systems, without the need for developing custom hardware.

The board can also be used for production flash programming on Mars modules, or for educational purposes.

This board is specially designed for image processing applications.

The main features of the Mars EB1 base board are:

- Support for USB 2.0 host
- FTDI USB 2.0 High-Speed device controller
- High-speed FPGA and flash programming over USB
- Versatile set of I/O connectivity options
- Ethernet RJ45 connector
- High-bandwidth and seamless operation with optional Enclustra FPGA Manager IP Solution [2]
- 2 × Mini Camera Link connectors[1]and HDMI 1.3 connector[1] ideal for image processing applications
- Easy fit with optional Enclustra Display Controller IP Core [3]
- microSD card slot
- Simple integration by using a single 12 V voltage supply
- Alternative power supply via USB device port
- Small solution size

1.1.2 Warranty

Please refer to the General Business Conditions, available on the Enclustra website [1].

1.1.3 RoHS

The Mars EB1 base board is designed and produced according to the Restriction of Hazardous Substances (RoHS) Directive (2011/65/EC).

1.1.4 Disposal and WEEE

The Mars EB1 base board must be properly disposed of at the end of its life. If a battery is installed on the board, it must also be properly disposed of.

The Waste Electrical and Electronic Equipment (WEEE) Directive (2002/96/EC) is not applicable for the Mars EB1 base board.

1.1.5 Safety Recommendations and Warnings

Mars boards are not designed to be "ready for operation" for the end-user. Proper configuration of the hardware before usage is required.

[1] Requires FPGA support (video protocol implementation)

Ensure that the power supply is disconnected from the board before inserting or removing a Mars module, connecting interfaces, or connecting jumpers.

Touching the capacitors of the DC-DC converters can lead to voltage peaks and permanent damage; over-voltage on power or signal lines can also cause permanent damage to the board and to the equipped module.

1.1.6 Electrostatic Discharge

Electronic boards are sensitive to electrostatic discharge (ESD). Please ensure that the product is handled with care and only in an ESD-protected environment.

1.1.7 Electromagnetic Compatibility

The Mars EB1 base board is a Class A product (as defined in IEC 61000-3-2 standard) and is not intended for use in domestic environments. The product may cause electromagnetic interference, for which appropriate measures must be taken.

1.2 Deliverables

- Mars EB1 base board
- Mars EB1 base board documentation, available via download:
  - Mars EB1 Base Board User Manual (this document)
  - Mars EB1 Base Board IO Net Length Excel Sheet [4]
  - Mars EB1 Base Board User Schematics (PDF) [5]
  - Mars EB1 Base Board Known Issues and Changes [6]
  - Mars EB1 Base Board 3D Model (PDF) [7]
  - Mars EB1 Base Board STEP 3D Model [8]
  - Mercury Mars Module Pin Connection Guidelines [9]

1.3 Accessories

- Mars FPGA or SoC module
- 12 V DC/2.5 A power supply
- USB 2.0 A to micro-B USB cable

2 Getting Started

This section contains essential information on using the Mars EB1 base board.

Electrostatic discharge (ESD) may damage the Mars EB1 base board partially or completely. Please follow the relevant guidelines for ESD-safe handling when operating or assembling electronic components.

Before first use of the Mars EB1 base board with a Mars module, the following steps must be followed:

- Mount the module on the module slot on the base board, with the power switched off.
- Set the DIP switches correctly (refer to Section 6.3).
- Set the I/O voltage selection jumpers correctly (refer to Section 5.5).
- Power up the board (refer to Section 5 for power options).

The power supply of the base board must be turned off in the following situations:

- Before changing the position of the I/O voltage selection jumpers
- Before removing the Mars module
- Before connecting or disconnecting peripherals to ANIOS and I/O connectors

Before connecting peripherals, make sure that the corresponding VCC_IO voltage is properly set.

The operating conditions for the Mars EB1 base board and equipped module must conform to the values given in Section 7, and in the relevant section from the Mars module user manual.

3 Board Description

3.1 Block Diagram

The Mars EB1 base board can be used in combination with any Mars module.

The block diagram of the Mars EB1 base board is shown in Figure 1.

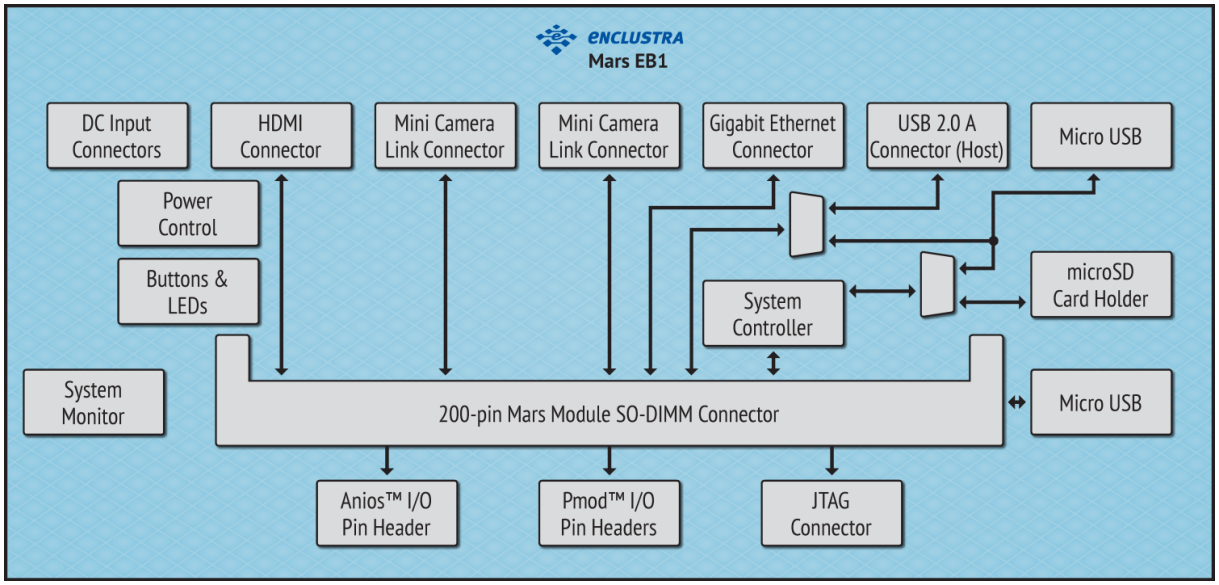

Figure 1: Hardware Block Diagram

3.2 Features

Table 1 describes the features available on the Mars EB1 base board.

Feature	Description
Form factor	120 × 80 mm
System features	System controller Built-in Xilinx JTAG (via USB connection) System monitor Power control Current sense
Memory	microSD card holder User EEPROM
Connectors	USB 2.0 host connector 2 × micro USB device connectors (one connector is shared with the USB 2.0 host) FTDI USB 2.0 High-Speed device controller RJ45 Gigabit Ethernet connector 2 × Mini Camera Link connectors[2] HDMI 1.3 connector[2]
User I/Os	40-pin Anios pin header 3× 12-pin pin headers (from which 2× Pmod™ compatible)
Supply voltage	12 V DC (internal, external) USB-power (with restrictions)

Table 1: Base Board Features

Warning!
Please note that the available features depend on the equipped Mars FPGA/SoC module.

3.3 Board Configuration and Product Models

Table 2 describes the standard base board configurations. Custom configurations are available; please contact Enclustra for further information.

[2] Requires FPGA support (video protocol implementation)

Product Model	Features	Temperature Range
MA-EB1-W	Refer to Table 1	-25..+85° C

Table 2: Standard Base Board Configurations

3.4 EN-Numbers and Part Names

Every board is uniquely labeled, showing the EN-number and serial number. An example is presented in Figure 2.

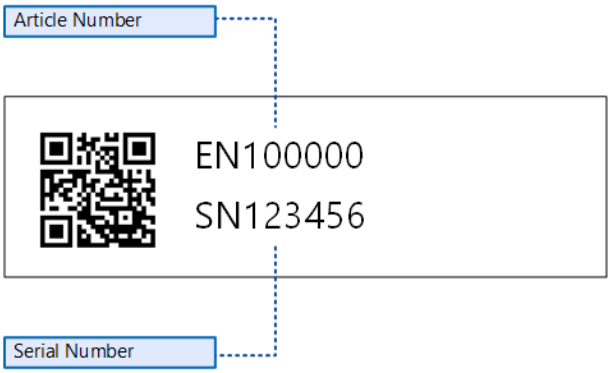

Figure 2: Product Label

The correspondence between EN-number and part name is shown in Table 3. The part name represents the product model, followed by the revision; the R suffix and number represent the revision number.

The revision changes and product known issues are described in the Mars EB1 Base Board Known Issues and Changes document [6].

EN-Number	Part Name
EN100785	MA-EB1-W-R1
EN100786	MA-EB1-C-R1
EN100861	MA-EB1-W-R2
EN100906	MA-EB1-C-R2
EN103052	MA-EB1-W-R2.5

Table 3: EN-Numbers and Part Names

3.5 Top and Bottom Views

3.5.1 Top View

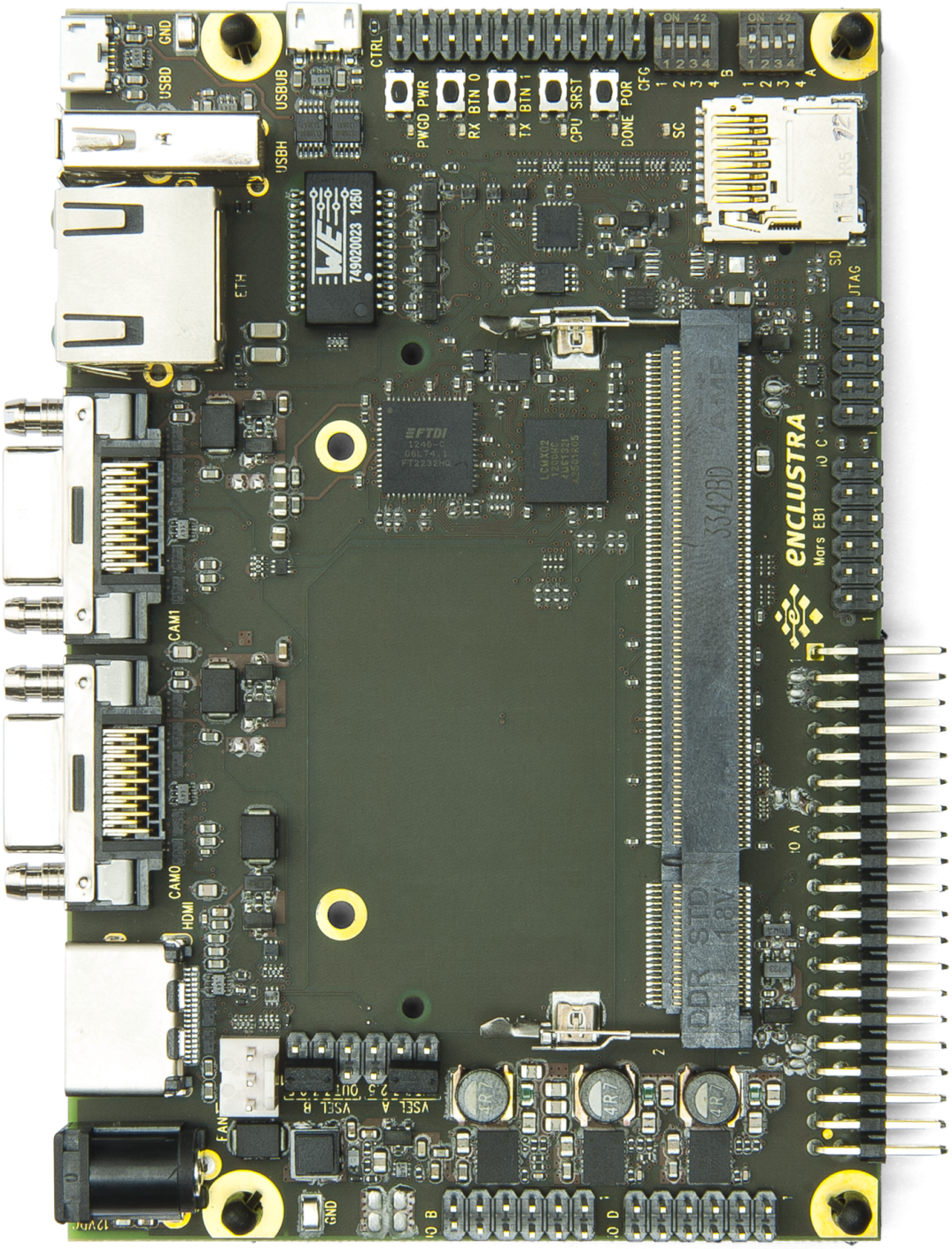

Figure 3: Board Top View

3.5.2 Bottom View

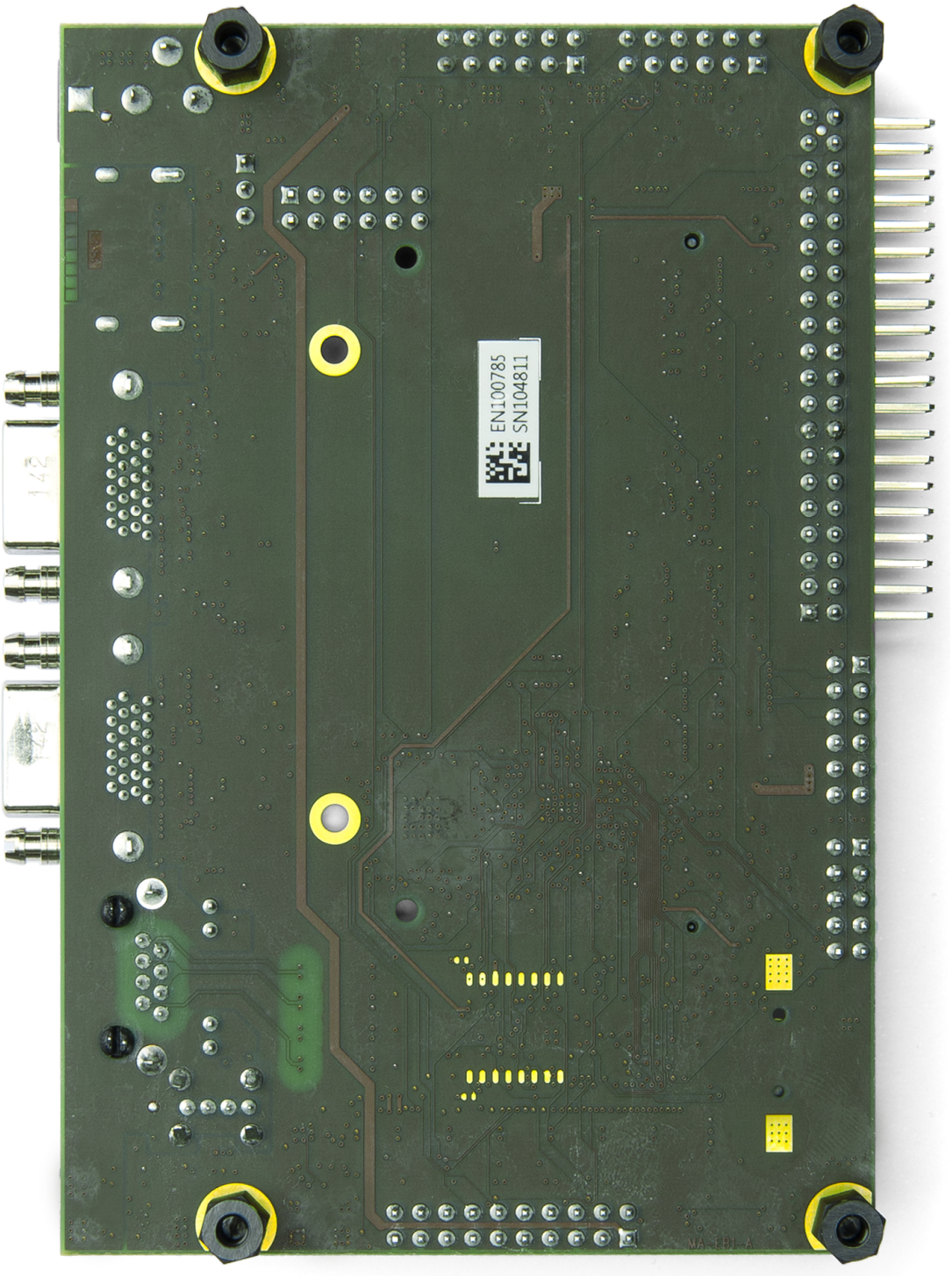

Figure 4: Board Bottom View

Please note that depending on the hardware revision and configuration, the base board may look slightly different than shown in this document.

3.6 Top and Bottom Assembly Drawings

3.6.1 Top Assembly Drawing

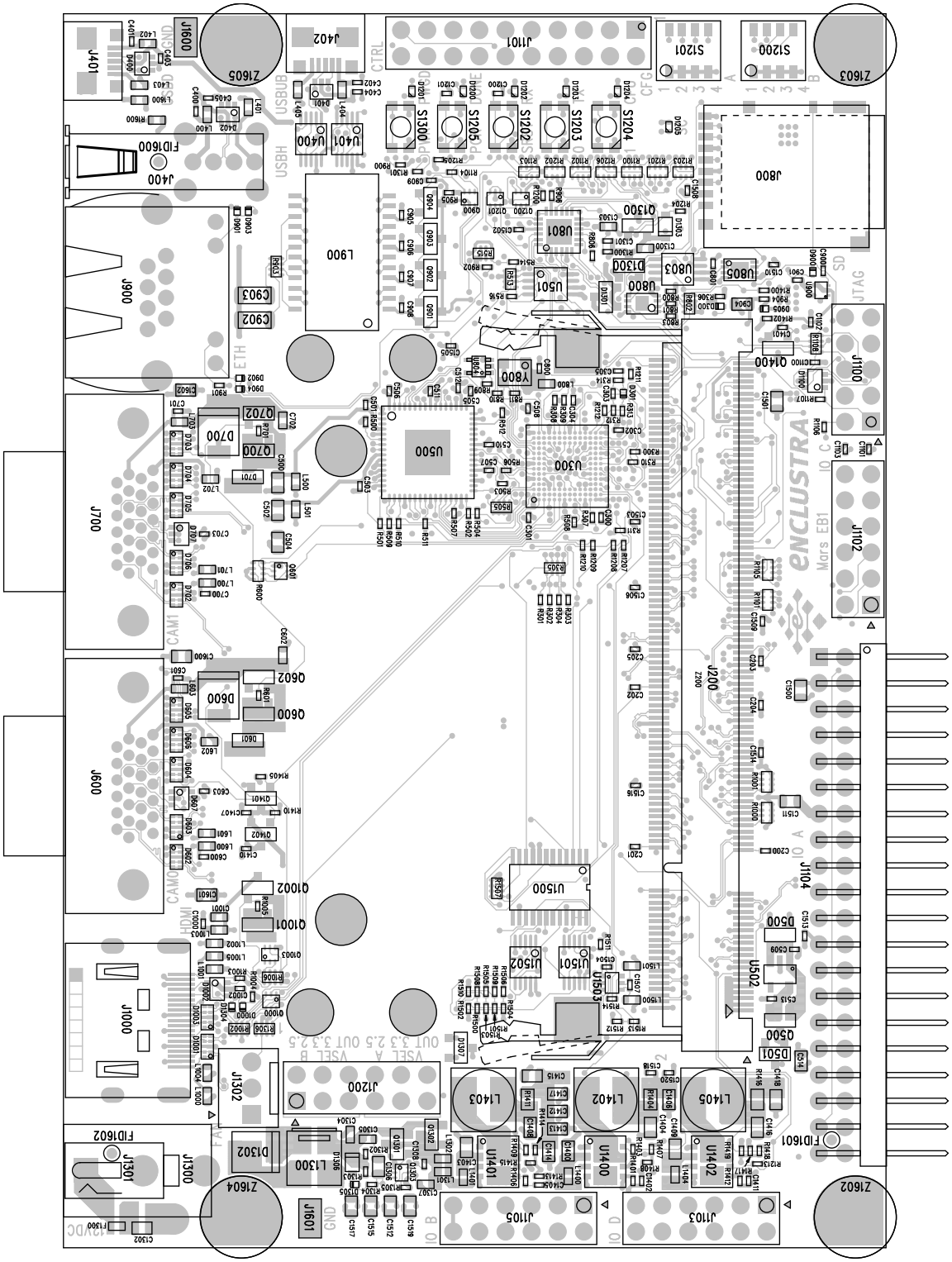

Figure 5: Board Top Assembly Drawing

3.6.2 Bottom Assembly Drawing

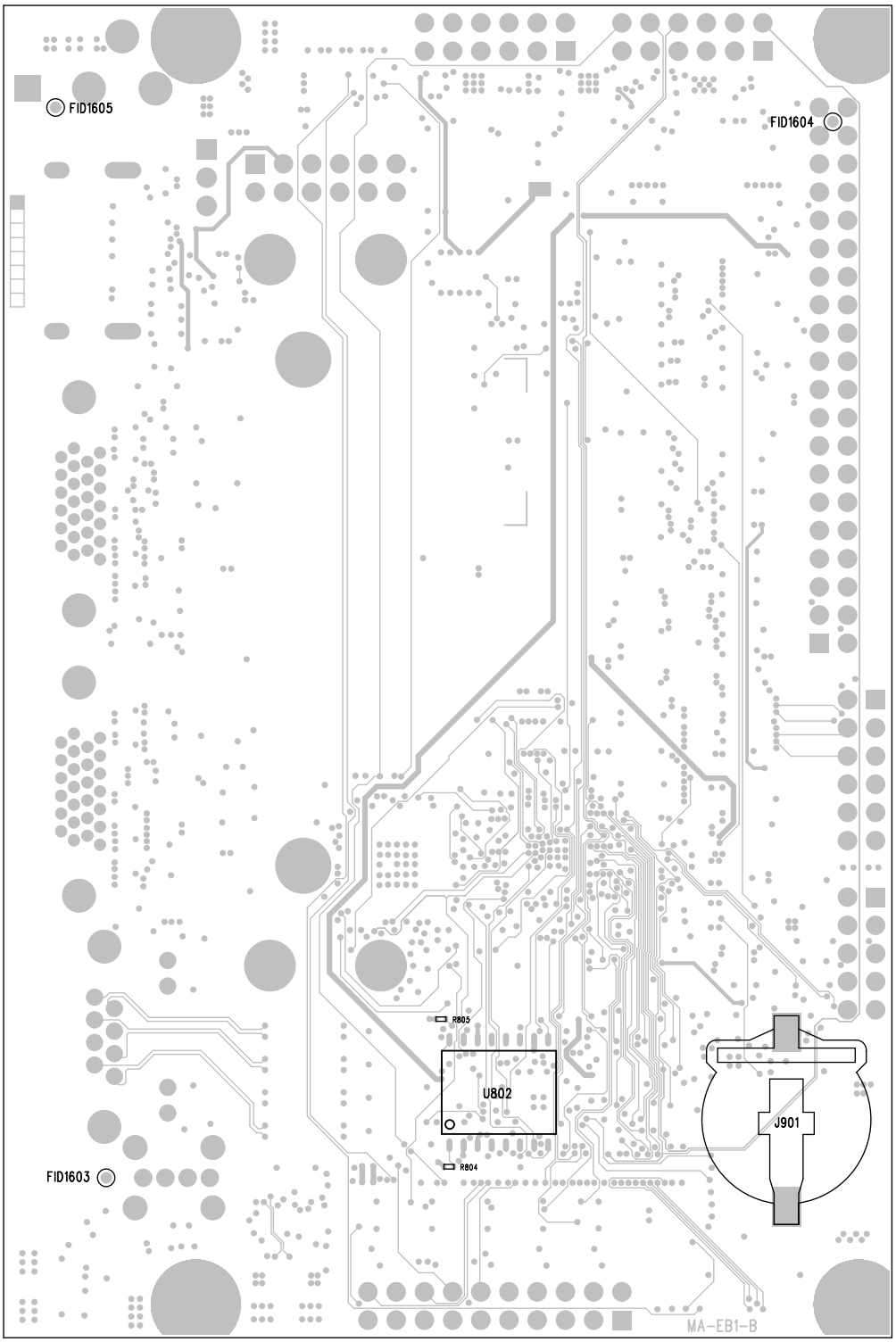

Figure 6: Board Bottom Assembly Drawing

Please note that depending on the hardware revision and configuration, the base board may look slightly different than shown in this document.

3.7 Board Dimensions

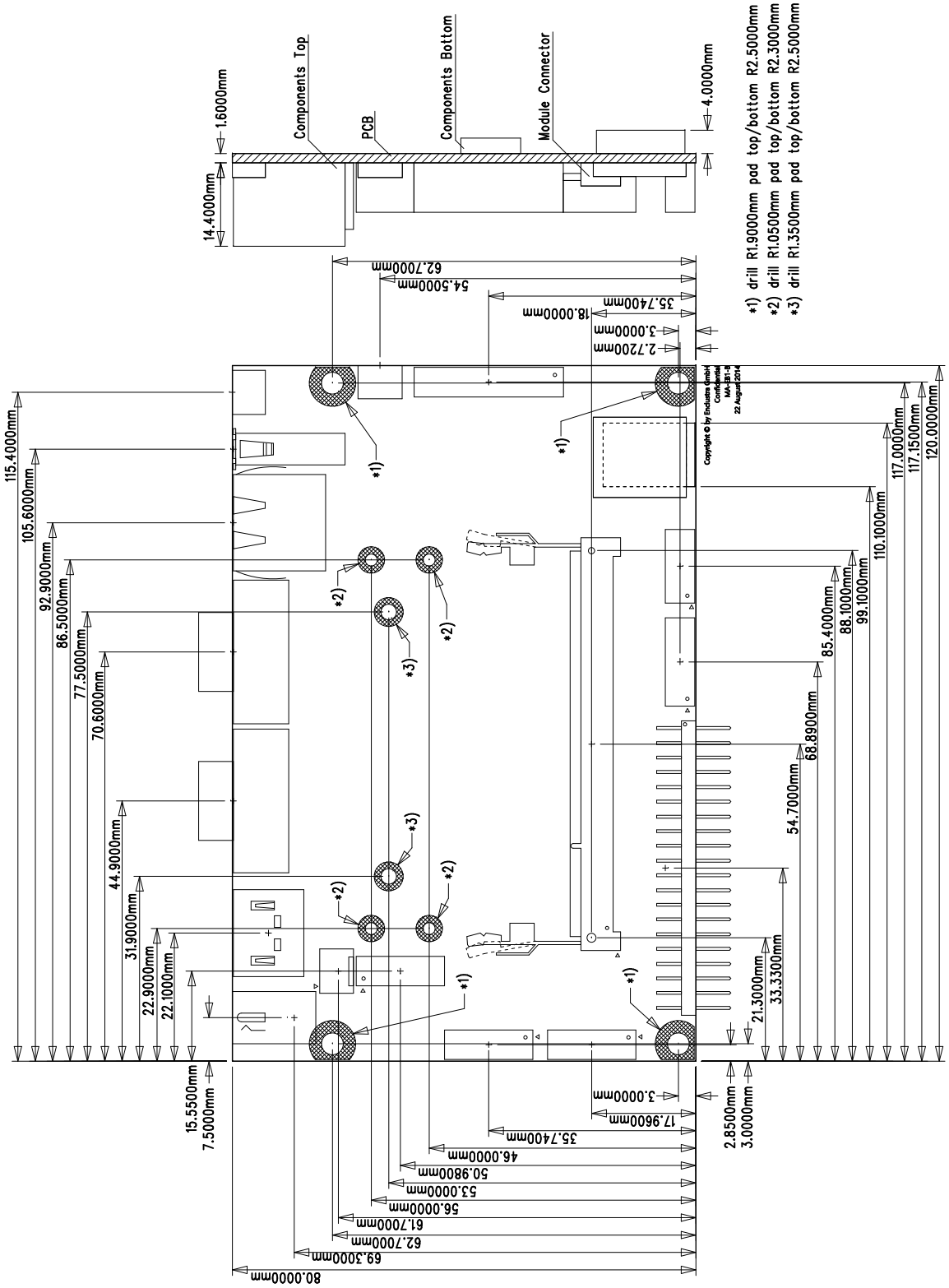

Figure 7: Board Dimensions

3.8 Mechanical Data

Table 4 describes the mechanical characteristics of the Mars EB1 base board. A 3D model (PDF) and a STEP 3D model are available [7], [8].

Symbol	Value
Size	120 × 80 mm
Component height top	14.4 mm
Component height bottom	4 mm
Weight	60 g

Table 4: Mechanical Data

3.9 Mechanical Components

Table 5 describes the mechanical components present on the Mars EB1 base board. The listed elements are for reference only. Any other components that meet the requirements may be used.

Product Number	Manufacturer	Description
973080365	Würth Elektronik	4 × plastic spacer bolt with female thread/clip, length 8 mm

Table 5: List of Mechanical Components

4 Connectors Description

4.1 12 V External Power (J1300)

This connector is used to supply the main VCC input voltage.

Apply only 12 V DC to this connector.

Pin Number	Signal Name	Description
1 (inner)	VCC_12V_IN	12 V DC (nominal) input voltage
2 (outer)	GND	Ground

Table 6: J1300 - External Power Connector

Type	Manufacturer
PJ-102AH	CUI Inc.

Table 7: J1300 - External Power Connector Type

The inner and outer diameters of the mating plug are 2.0 mm and 5.5 mm respectively.

4.2 Fan/12 V Internal Power Connector (J1302)

The Mars EB1 base board can alternatively be powered through the internal power input connector. The 12 V DC power source connected to J1302 must be filtered by external power circuitry.

If the external power input is used, this connector can be used to equip a 12 V fan with a sense signal to the Mars EB1 base board.

Pin Number	Signal Name	Description
1	GND	Ground
2	VCC_MAIN	12 V DC (nominal) input voltage
3	SYSMON_TACHO	Sense signal to determine fan speed. See Section 6.7 for details

Table 8: J1302 - Fan/Internal Power Connector

Type	Manufacturer
61900311121	Würth Elektronik

Table 9: J1302 - Fan/Internal Power Connector Type

Warning!

Do not short circuit the 12 V power supply, and make sure the currents flowing through the pins of this connector do not exceed 2.0 A. Otherwise, the PCB may be damaged.

Table 10 shows an example of a mating part for the fan/internal power connector.

Type	Manufacturer
61900311621	Würth Elektronik

Table 10: Mating Part for the Fan/Internal Power Connector

4.3 I/O Voltage Selection (J1200)

The I/O voltage selection jumpers are used to configure the VCC_IO_A and VCC_IO_B voltages that power the I/O banks of the SoC/FPGA device on the Mars module. Refer to Section 5.5 for details.

4.4 Mars Module Connector (J200)

A detailed pinout of the Mars module connector can be found in the Mars Master Pinout [10] and in the Mars EB1 Base Board User Schematics [5].

Table 11 indicates the module connector type.

Height	Type	Type
5.2 mm	TE 1565917-4	TE Connectivity

Table 11: Module Connector Type

Warning!

Only Enclustra Mars FPGA/SoC modules should be inserted into the Mars EB1 base board.

Warning!

The VCC_IO pins are directly connected to the FPGA/SoC device. Apply only compliant voltages to the VCC_IO pins; any other voltage may damage the mounted Mars FPGA/SoC module, as well as other devices on the Mars EB1 base board.

4.5 USB 2.0 Host Connector (J400)

If the mounted Mars module features a USB controller, the module's USB signals can be connected to J400 via a multiplexer. Details on USB connections on the board are available in Section 6.5.

The power and data signals on this connector are ESD-protected.

4.6 Micro USB 2.0 Device Connectors (J401/J402)

There are two micro USB 2.0 device connectors on the Mars EB1 base board: one on the front panel and one on the side.

The micro USB connector on the side can be connected to the on-board FTDI device, and the micro USB on the front panel can be either connected to the FTDI device, or to the USB signals coming from the module connector. The configuration is done by changing the position of the DIP switches - refer to Sections 6.5 and 6.3 for details.

The base board can be powered via any of the micro USB 2.0 device connectors; further information on USB power is available in Section 5.2.

The power and data signals on J401/J402 connectors are ESD-protected.

4.7 Gigabit Ethernet Port (J900)

The Mars EB1 base board is equipped with a 10/100/1000 Mbit Ethernet port. The capability of the Ethernet interface depends on the connected Mars module.

The RJ45 connector J900 is connected through magnetics directly to the Mars module connector. For details on the Ethernet interface, refer to Section 6.4.

4.8 Mini Camera Link Connectors (J600/J700)

The Mars EB1 base board is equipped with two Mini Camera Link connectors. The signals available on these connectors are routed directly to/from the FPGA banks on the SoC/FPGA device on the Mars module.

Power over Camera Link (POCL) for the two connectors can be activated via two enable signals: PWR_EN_CAM0 and PWR_EN_CAM1. These signals can be toggled by writing the corresponding registers in the system controller - refer to section 6.10 for details. By default, the power over Mini Camera Link is not active.

The signals on the connectors have no termination resistors and they are ESD-protected.

The pinout on the J600/J700 connectors corresponds to the Mini Camera Link standard maintained by AIA (Automated Imaging Association). In order to receive and transmit video signals through the links, FPGA support is required (video protocol implementation).

4.9 HDMI Connector (J1000)

The Mars EB1 base board is equipped with an HDMI connector. The signals available on this connector are routed directly to/from the FPGA banks on the SoC/FPGA device on the Mars module.

The power connection for the HDMI is activated by an enable signal: PWR_EN_HDMI. This signal can be activated by writing the corresponding register in the system controller - refer to section 6.10 for details. By default, the power over HDMI is not active.

The signals on this connector have 50 Ω termination resistors to VCC_IO_B and are ESD-protected.

The I2C communication on the HDMI connector is currently not supported. The I2C connectivity circuits present in the board schematics are intended for future use.

The pinout on the J1000 connectors corresponds to the HDMI standard. In order to receive and transmit video signals through the links, FPGA support is required (video protocol implementation).

The Enclustra Display Controller IP Core [3] can be easily integrated into any user design and facilitates the development of FPGA video applications.

4.10 microSD Card Slot (J800)

The enclosure of J800 is connected to GND.

The microSD card signals can be connected via a multiplexer with a built-in level shifter to the Mars module SDIO signals. This signal path can be activated by setting the SDIO_SEL signal to logic high. This signal is controlled by the DIP switch CFG A 3 or by the system controller. Refer to Sections 6.3 and 6.10 for details on configuration.

4.11 Anios I/O Connector A (J1104)

The Anios I/O connector can be used for user applications: it provides 24 user I/Os, a differential clock connection, connectivity to the I2C bus, and power supply connections. The clock, data and I2C signals are routed to the module connector - for details, refer to the Mars EB1 Base Board User Schematics [5].

Warning!

The Anios I/O pins are connected directly to the FPGA/SoC device. Use only VCC_IO voltages compliant with the equipped FPGA/SoC device; any other voltage may damage the mounted Mars FPGA/SoC module, as well as other devices on the Mars EB1 base board.

4.12 PMOD I/O Connectors B, C (J1102/J1105)

The dual PMOD I/O connectors (2 × 6) can be used for user applications: each connector provides 8 user I/Os and power supply connections. The signals on PMOD B are connected directly to the module connector, while the signals on PMOD C are connected via 100 Ω series resistors to the module connector and in parallel to the system controller and to the on-board user buttons. For details, refer to the Mars EB1 Base Board User Schematics [5].

The PMOD I/O connector B is Digilent Pmod™ compatible when VCC_IO_B is 3.3 V.

The PMOD I/O connector C is Digilent Pmod™ compatible when VCC_IO_A is 3.3 V.

Warning!

The PMOD I/O pins are connected directly to the FPGA/SoC device. Use only VCC_IO voltages compliant with the equipped FPGA/SoC device; any other voltage may damage the mounted Mars FPGA/SoC module, as well as other devices on the Mars EB1 base board.

Warning!

Do not insert a PMOD module to these connectors if the corresponding VCC_IO_[x] supply is not 3.3 V, as this may damage the mounted Mars FPGA/SoC module, as well as other devices on the Mars EB1 base board.

4.13 I/O Connector D (J1103)

The signals on I/O connector D can be used for user applications and/or for connecting an MMC interface to the SDIO pins. The MMC signals are activated by setting the CFG A 3 switch. Refer to Section 6.3 for details.

Warning!

Some of the I/O pins on this connector are routed directly to the FPGA/SoC device. Use only VCC_IO voltages compliant with the equipped FPGA/SoC device; any other voltage may damage the mounted Mars FPGA/SoC module, as well as other devices on the Mars EB1 base board.

4.14 Battery Holder (J901)

The battery holder and battery are not mounted in the standard configuration of the Mars EB1 base board. The battery on the Mars EB1 base board is used for buffering the real-time clock on the connected Mars FPGA/SoC module. If required, a 3 V lithium battery (CR1220) can be used.

Alternatively, the VCC_BAT_IN power signal can be driven via pin 6 of connector J1101. Refer to Section 4.16 for details.

Type	Manufacturer
BC501SM	Memory Protection Devices

Table 12: J901 - Battery Holder Type

Warning!

There is a danger of explosion if the battery is replaced incorrectly - only replace the battery with the same or equivalent type recommended by Enclustra.

Used batteries should be disposed of according to the manufacturer's instructions.

4.15 FPGA JTAG Connector (J1100)

The FPGA JTAG connector allows accessing the JTAG port of the mounted Mars FPGA/SoC module. The signals on this connector are protected against ESD. Series termination resistors are equipped between the module signals and the JTAG header.

Pin Number	Connection	Series Resistor
1	JTAG_TCK	22 Ω
2	JTAG_PRESENT#	1 kΩ
3	JTAG_TDO	100 Ω
4	VCC_IO_A	
5	JTAG_TMS	100 Ω
6	SRST#_RDY	100 Ω
7, 8	Not connected	
9	JTAG_TDI	100 Ω
10	GND	

Table 13: J1100 - FPGA JTAG Connector

JTAG_PRESENT# is used to determine if an external JTAG adapter is connected; the external adapter should tie this signal to GND when the cable is plugged in.

Warning!

The JTAG pins are connected to the FPGA/SoC device via small-value series resistors. Use only VCC_IO voltages compliant with the equipped FPGA/SoC device. Any other voltages may damage the equipped FPGA/SoC device as well as other devices on the module or Mars EB1 base board.

The JTAG connector available on the Mars EB1 base board can be used in combination with Xilinx Platform Cable USB or Intel USB-Blaster download cable. For Xilinx JTAG connection, the flying wire adapter must be used. For Intel JTAG connection, the download cable can be connected directly to the on-board JTAG connector, as the pinout matches the Intel USB-Blaster pinout.

4.15.1 Xilinx JTAG over System Controller

The system controller includes built-in Xilinx JTAG programmer functionality, making it possible to use a USB connection for JTAG debugging. It is fully supported by the Xilinx tools.

The following steps need to be taken in order to use the Xilinx JTAG:

- Set the FTDI device in Xilinx JTAG mode using the Enclustra Module Configuration Tool (MCT) [11]
- Set the ScMode0 register to 0 (refer to Sections 6.3 and 6.10)
- Set the USB_SEL signal so that the currently used USB connector is routed to the FTDI device (refer to Sections 6.3 and 6.5)

4.15.2 Intel JTAG over System Controller

Currently, the built-in Intel JTAG functionality is not supported by the system controller.

4.16 Control Connector (J1101)

The control connector is used mainly for control and monitoring purposes. Many different control functions are affected by the signals connected to this connector. Detailed information is available in Table 14.

Pin Number	Signal Name	Description	Function
1	VCC_12V_CM	12 V DC main voltage	Supply output/ Monitor
2	GND	Ground	-
3	VCC_5V	5 V DC-DC converter output	Supply output/ Monitor
4	VCC_3V3_SC	3.3 V DC voltage for the system controller power	Monitor
5	UART_RX_EXT	External connection UART RX, configurable via system controller registers See Section 6.10 for details	Control
6	VCC_BAT_IN	External connection for battery supply	Supply input/ Monitor
7	UART_TX_EXT	External connection UART TX, configurable via system controller registers See Section 6.10 for details	Control
8	PWR_GOOD	Power good status	Monitor
9	PWR_BTN#	External connection for power button	Control
10	PWR_EN	Power enable status	Control
11	GND	Ground	-
12	FTDI_BDBUS7_SCJTAGEN	Reserved for internal use	-
13	SYSMON_GPI	General purpose input to the system monitor	Control
14	FTDI_BDBUS0_SCTCK_TXD	Reserved for internal use	-
15	SYSMON_GPO#	General purpose output from the system monitor	Monitor
16	FTDI_BDBUS1_SCTDI_RXD	Reserved for internal use	-
17	POR#_LOAD#	External connection for power-on reset signal	Control
18	FTDI_BDBUS2_SCTDO	Reserved for internal use	-
19	FPGA_DONE	FPGA configuration done status	Monitor
20	FTDI_BDBUS3_SCTMS	Reserved for internal use	-

Table 14: J1101 - Control Connector

5 Power

5.1 Power Input

The Mars EB1 base board can be powered using one of the power input sources listed below:

- External power connection through J1300 connector
- Internal power connection through J1302 connector
- USB VBUS power connection

5.2 Power over USB

As soon as a USB cable is plugged into the Mars EB1 base board, the system controller and the FTDI USB 2.0 device controller are powered over USB; this will cause the SC LED to blink.

If external USB power is enabled, the Mars EB1 base board and the mounted Mars module are powered over USB. In this case, VCC_MAIN is connected to the USB input voltage. Table 15 describes the VBUS power control; the factory default is marked in bold.

DIP Switch CFG A 2	USB_PWR_EN#	Effect
OFF	**1**	**USB power is not connected to the VCC_MAIN domain. An external 12 V supply must be connected to the board.**
ON	0	USB power (5 V) is connected to VCC_MAIN domain. The Mars EB1 base board is powered via the USB connector (J401 or J402).

Table 15: USB - VBUS Control

Warning!
If the Mars module is powered via USB, make sure that it does not consume more power than the USB specification allows.

5.3 Power Control

Power control is enabled and disabled by the PWR_ON# signal, determined by the position of the DIP switch CFG A 4. Table 16 describes the power control configuration; the factory default is marked in bold.

DIP Switch CFG A 4	PWR_ON#	Effect
OFF	1	Power control is ON
ON	**0**	**Power control is OFF**

Table 16: Power Control Switch Configuration

If power control is disabled, the Mars EB1 base board and the mounted module are powered as soon as power is applied through external or internal power connectors.

If power control is enabled, the Mars module is not powered, even when power is applied to the Mars EB1 base board. By pressing the power button (PWR) for a short time, the power is turned on. Power can be turned off again by pressing the power button for a configurable time. Power can also be turned on and off by writing a system controller register - see Section 6.10 for more information.

Power control is not available when power over USB is active.

5.4 Power Sequencing

The on-board VCC_3V3 power domain is switched on when all the power supplies on the module and board are within their range (PWR_GOOD signal is high).

PWR_GOOD	Effect
0	VCC_3V3 domain is switched off
1	VCC_3V3 domain is switched on

Table 17: Power Sequencing

5.5 I/O Voltage Selection

The I/O voltage selection jumpers are used to configure the VCC_IO_A and VCC_IO_B voltages that power the I/O banks of the SoC/FPGA device on the Mars module.

Tables 18 and 19 describe the usage of jumpers. Please note the following:

- VCC_OUT is a supply output from the Mars module. The value of the voltage depends on the mounted Mars module (Refer to the "Voltage Supply Outputs" Section in the Mars module user manual).
- Only one jumper per VCC_IO_A, respectively VCC_IO_B is allowed (one choice per table)
- The factory default jumper settings are 2-4 and 8-10. As a consequence of these settings, no voltage is applied to the Mars module connector, therefore it prevents the module from booting. PWGD LED will not be lit.

Figure 8 shows the pin numbering for connector J1200 and one configuration example.

Jumper	Position	Function	Description
J1200	7-8	VCC_2V5 selected	VCC_2V5 is connected to VCC_IO_A
J1200	9-10	VCC_3V3 selected	VCC_3V3 is connected to VCC_IO_A
J1200	11-12	VCC_OUT selected	Module VCC_OUT is connected to VCC_IO_A

Table 18: Jumper Settings VCC_IO_A

Jumper	Position	Function	Description
J1200	1-2	VCC_2V5 selected	VCC_2V5 is connected to VCC_IO_B
J1200	3-4	VCC_3V3 selected	VCC_3V3 is connected to VCC_IO_B
J1200	5-6	VCC_OUT selected	Module VCC_OUT is connected to VCC_IO_B

Table 19: Jumper Settings VCC_IO_B

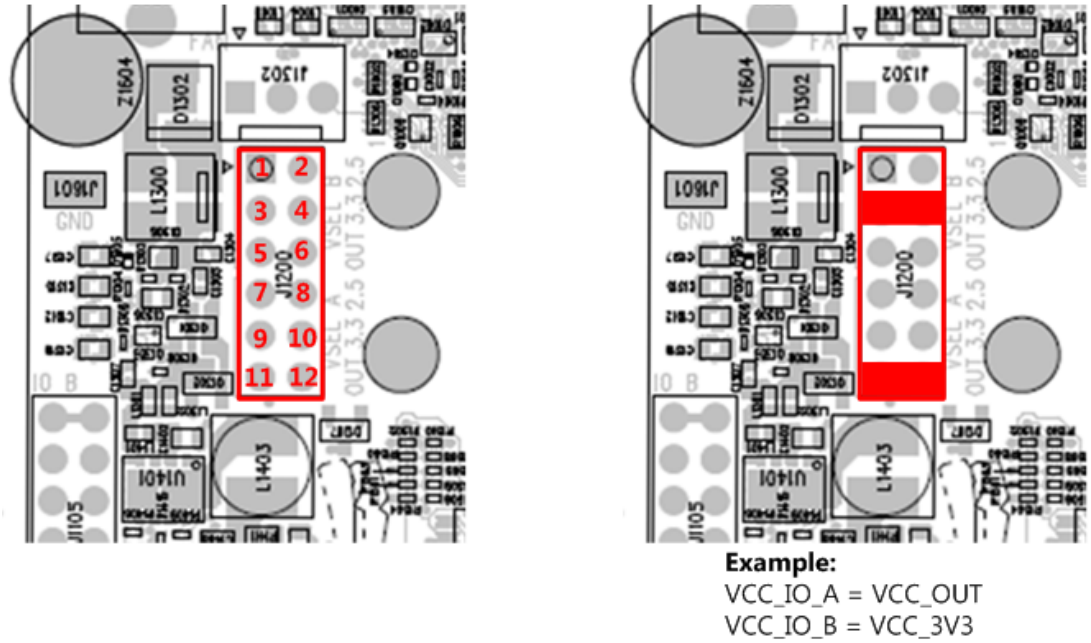

Figure 8: VCC_IO Jumper Positions - Pin Numbering and Configuration Example

6 Board Function

6.1 LEDs

LED Name	LED	Signal Name	Controlled by	Description
PWGD	D1201	PWR_OK#	Power circuits	Indicates that PWR_GOOD is active and VCC_IO_A and VCC_IO_B are available
DONE	D1200	FPGA_DONE	Power circuits	FPGA configuration is done
RX	D1202	NOR_MISO_RXLED#	System controller	UART RX status, shared with SPI NOR flash MISO signal
TX	D1203	NOR_MOSI_TXLED#	System controller	UART TX status, shared with SPI NOR flash MOSI signal
CPU	D1204	NOR_CLK_CPULED#	System controller	CPU status, shared with SPI NOR flash CLK signal
SC	D1205	NOR_CS#_SCLED#	System controller	System controller status, shared with SPI NOR flash CS signal

Table 20: Board LEDs

For details on the LED connections, refer to Section 6.10 and to the Mars EB1 Base Board User Schematics [5].

6.2 Buttons

All buttons are active-low; their function is described in Table 21.

The user buttons can be configured by the user to have various functions. For details, refer to Section 6.10 and to the Mars EB1 Base Board User Schematics [5].

Button Name	Button	Signal Name	Function	Comments
PWR	S1300	PWR_BTN#	Power on/off	Refer to Section 5.3
POR	S1205	POR#_LOAD#	Power-on reset/ Configuration-clear	Refer to the Enclustra Module Pin Connection Guidelines [9]
SRST	S1202	SRST#_RDY#	Soft-reset/ Configuration-delay	Refer to the Enclustra Module Pin Connection Guidelines [9]
0	S1203	IOC_D0_SC0_BTN0#	User function	Shared with the system controller, module connector and PMOD I/O connector C
1	S1204	IOC_D1_SC1_BTN1#	User function	Shared with the system controller, module connector and PMOD I/O connector C

Table 21: Board Buttons

6.3 DIP Switches

There are two configuration switches on the Mars EB1 base board: CFG A and CFG B. Tables 22 and 23 describe their function; the factory default is marked in bold.

For details on the board configuration, refer to the Mars EB1 Base Board User Schematics [5].

DIP Switch	Signal Name	Pos.	Effect	Comments
CFG A 1	BOOT_MODE0	OFF	BOOT_MODE0 is set to 1	Refer to the Mars module user manual
		ON	**BOOT_MODE0 is set to 0**	
CFG A 2	USB_PWR_EN#	**OFF**	**Power over USB OFF**	Refer to Section 5.2
		ON	Power over USB ON	
CFG A 3	SDIO_SEL	**OFF**	**SD card active**	SDIO_SEL is set to 1: the SDIO signals from module connector are routed to the SD card
		ON	MMC pins active	SDIO_SEL is set to 0: the SDIO signals from module connector are routed to the MMC pins
CFG A 4	PWR_ON#	OFF	Power control ON	Refer to Section 5.3
		ON	**Power control OFF**	

Table 22: S1201 - Configuration Switch A

DIP Switch	Signal Name	Pos.	Effect	Comments
CFG B 1	USBMOD_ID	OFF	The module USB signals are routed to the micro USB connector (front panel)	Refer to Section 6.5
		ON	**The module USB signals are routed to the USB host connector**	
CFG B 2	USB_SEL	**OFF**	**On startup: BOOT_MODE1 is set to 1**	Refer to Section 6.5
			After startup: The FTDI signals are routed to the micro USB connector (on side)	
		ON	On startup: BOOT_MODE1 is set to 0	
			After startup: The FTDI signals are routed to the micro USB connector (front panel)	
CFG B 3	VMON_SEL_SCMODE0#	**OFF**	**On startup: ScMode0 register is set to 1**	Refer to Sections 6.10 and 6.7
			After startup: VMON_SEL is set to 1	
		ON	On startup: ScMode0 register is set to 0	
			After startup: VMON_SEL is set to 0	
CFG B 4	SCMODE1#	**OFF**	**No function (reserved for future use)**	Refer to Section 6.10
		ON	No function (reserved for future use)	

Table 23: S1200 - Configuration Switch B

Warning!

The switch configuration CFG B 1 OFF and CFG B 2 ON is not permitted, and may damage the Mars EB1 base board and equipped Mars module.

Some of the configuration switches have different functions, on startup and after startup; these switches are connected to the system controller, which reads the switch positions on startup and defines the behavior of certain circuit elements accordingly.

When powering the system controller, the switch has the "On startup" effect; afterwards the switch can be toggled to obtain the required hardware configuration.

Note that the system controller is powered when either a USB cable is attached, or when the main power is applied. For example, if the application requires that BOOT_MODE1 is set to 1 and that the FTDI signal is routed to the micro USB connector (front panel), the user should follow these steps:

- Disconnect the power supply from the board
- Disconnect all USB cables from the board
- Configure the DIP switches for the desired boot mode

- Plug the USB cable into the micro USB connector (front panel) (in order to power up the system controller, so that the "On startup" switch setting is latched)
- Configure the DIP switches for the FTDI path routing
- Power up the board using 12 V DC

Please refer to Section 6.10 for details on system controller inputs that are read at startup.

Table 24 describes the meaning of the ScMode0 register and its influence on the Mars EB1 base board functionality. The ScMode0 register of the system controller can also be configured using I2C - refer to Section 6.10 for details.

ScMode0 Register	Effect
0	The system controller has Xilinx JTAG functionality
1	The system controller has Intel JTAG functionality (currently not supported)

Table 24: ScMode0 Register Usage

6.4 Ethernet

The Mars EB1 base board is equipped with a Gigabit Ethernet port, configured according to the capabilities of the mounted module.

The Ethernet magnetics and the RJ45 connector are equipped on the base board, while the Ethernet PHY is equipped on the Mars module.

The Ethernet port on the Mars EB1 base board can be used as 1 Gigabit Ethernet port or as 2 × 10/100 Mbit Ethernet ports, depending on the equipped Mars module. If the RJ45 connector on the board is used for a dual Fast Ethernet implementation, an external RJ45 Y-adapter/splitter is required in order to convert the 4-pairs connection into 2 × 2-pairs connections.

6.5 USB

6.5.1 USB Overview

Figure 9 presents an overview of the USB connections on the Mars EB1 base board. The default configuration is marked in bold.

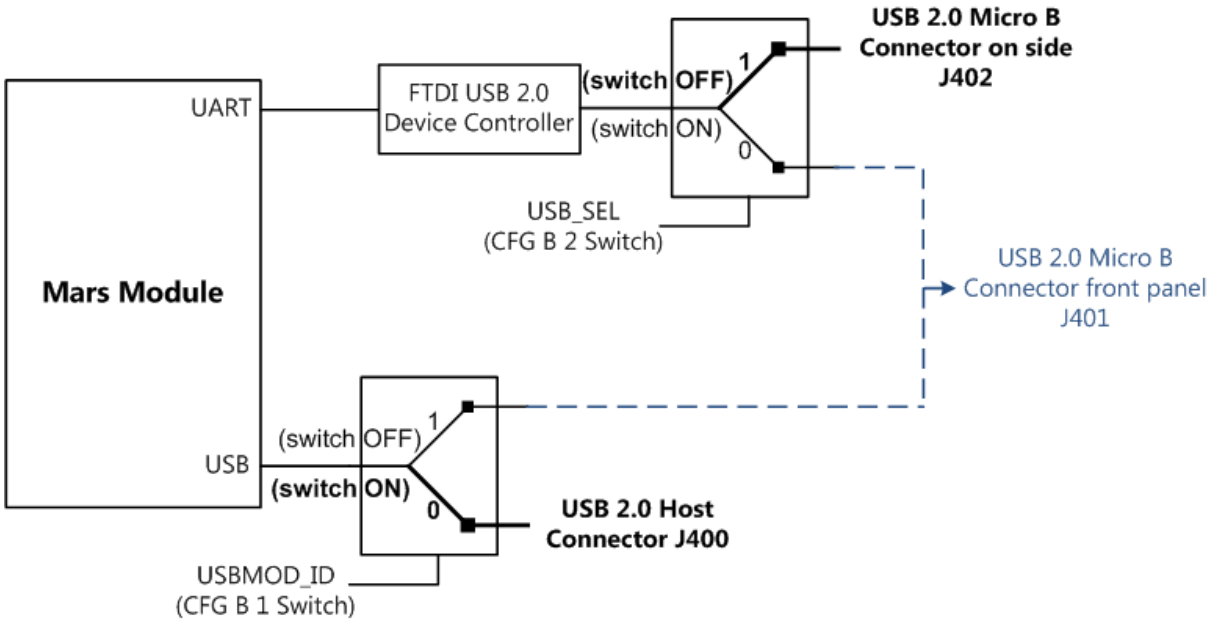

Figure 9: USB Connections Overview

The FTDI device can be connected either to the USB 2.0 micro B connector on the front panel, or to the USB 2.0 micro B connector on the side. The FTDI connection can be used for configuration or test purposes.

Warning!

The switch configuration CFG B 1 OFF (activate connection from module USB to USB 2.0 micro B front panel connector) and CFG B 2 ON (activate connection from FTDI to USB 2.0 micro B front panel connector) is not permitted, and may damage the Mars EB1 base board and equipped Mars module.

6.5.2 USB 2.0 Device Controller (FTDI)

The FTDI FT2232HQ USB 2.0 device controller present on the Mars EB1 base board can be used to easily implement a communication link to a host PC.

The FTDI device is connected to the system controller and can be used for various communication protocols. Details on the FTDI modes and configuration can be found in Section 6.10.

By default, the UART communication between the FTDI device and FPGA is active. The Xilinx JTAG mode can be activated using the Enclustra MCT [11] and is independent of the UART connection.

The library used by the MCT is available free of charge; it allows users to integrate module enumeration, FPGA and SPI flash configuration, and I2C communication functionality in their own application. The library consists of a Windows DLL with a C-style interface, allowing use of the library from almost any programming language; for C++ applications, a C++ wrapper is also provided. Please contact Enclustra for details.

6.6 I2C Communication

There are several I2C devices on the Mars EB1 base board, connected to the I2C communication lines. These are presented in Table 25.

Note that the I2C signals connected to the Mars connector address other I2C devices equipped on the Mars module.

Board Reference	Function	I2C Address (7-bit)	Comments
J200	Mars module	-	Additional devices are available on the Mars module
U300	System controller	0x0D	
U1500	System monitor	0x2F	
U800	User EEPROM	0x57	
J1104	Anios I/O connector A	User-defined	

Table 25: I2C Bus System

The following device can be addressed using I2C if it has been previously activated by the signal I2C_EN_HDMI. This signal can be toggled by setting a system controller register. Refer to Section 6.10 for details.

BoardReference	Function	I2C Address
J1000	HDMI interface	User-defined

Table 26: I2C_EN_FMC Controlled Functions

6.7 System Monitor/Current Sense

The Mars EB1 base board features a system monitor and current sense circuit, addressable via I2C - these are used for voltage and current monitoring. Additional functionality, such as GPIO and fan control, is also available.

Type	Manufacturer
LM96080	Texas Instruments

Table 27: System Monitor Type

The system monitor performs two sets of voltage and current measurements. The user can select which set of inputs should be measured by toggling the value of the VMON_SEL signal. This can be set via DIP switches, or via the system controller registers. Please refer to Sections 6.3 and 6.10 for details.

Table 28 lists the voltage measurements performed by the system monitor.

Board Reference	Signal Name	System Monitor Register	VMON_SEL	Comments
-	VMON_MAIN	IN0	0	5 - 12 V
-	VMON_3V3	IN1	0	3.3 V ±5%
-	VMON_OUT	IN2	0	VCC_OUT voltage of the module (module dependent)
-	VMON_2V5	IN3	0	2.5 V ±5%
J200.41	VMON_P41	IN0	1	Module dependent
J200.42	VMON_P42	IN1	1	Module dependent
J200.94	VMON_P94	IN2	1	Module dependent
J200.198	VMON_P198	IN3	1	Module dependent
-	VMON_5V	IN4	- (don't care)	5 V ±10%
-	VMON_CS_MOD	IN5	- (don't care)	VCC_3V3_MOD current
-	VREF_CS	IN6	- (don't care)	VREF current sensor

Table 28: System Monitor Voltage Connections

Table 29 describes the GPIO and fan connections of the system monitor.

Board Reference	Signal Name	System Monitor Register	Description
J1302.3	SYSMON_TACHO	FAN1	Fan speed sense signal
J1101.13	SYSMON_GPI	GPI(CI)	General purpose input
J1101.15	SYSMON_GPO#	GPO#	General purpose output

Table 29: System Monitor I/O and Fan Connections

6.8 User EEPROM

The Mars EB1 base board features a user EEPROM which may be accessed via I2C. It can be used to store user data (e.g. a serial number) and can be accessed by the FPGA and by the system controller.

Type	Manufacturer
24AA128T-I/MNY	Microchip

Table 30: User EEPROM Type

6.9 SPI NOR Flash

The SPI NOR flash is not equipped in the standard configuration of the Mars EB1 base board. The current system controller firmware does not support communication between the SPI NOR flash and the Mars module.

6.10 System Controller

The Mars EB1 base board is equipped with a Lattice CPLD, LCMXO2-4000HC, with the role of a system controller managing the default function of the board and providing additional functions required to operate various interfaces.

Table 31 describes the system controller firmware versions programmed on the Mars EB1 base board. The listed zip archives are available on the Enclustra download page.

Revision	System Controller Firmware Version	Documentation and Upgrade Instructions
R1-R2	Mars_EB1-R2_System_Controller_Upgrade.zip	Included in the .zip archive (I2C registers documentation partially available in the old Mercury PE1 User Manual (R1-R3))
R2.5 and newer	Mars_EB1-R2-5_System_Controller_Upgrade.zip	Included in the .zip archive

Table 31: System Controller Firmware Versions

Please refer to the Mars EB1 Base Board Known Issues and Changes [6] document for details on the system controller firmware update on revision R2.5.

Contact Enclustra support for further information.

7 Operating Conditions

7.1 Absolute Maximum Ratings

Table 32 indicates the absolute maximum ratings for Mars EB1 base board.

Symbol	Description	Rating	Unit
VCC_12V_IN	Supply voltage relative to GND	-0.5 to 16	V
VCC_IO_[x]	VCC I/O input voltage relative to GND	Refer to the Mars module user manual	
$T_{ambient}$	Ambient temperature range for commercial boards (C) *	0 to +70	°C
	Ambient temperature range for wide range boards (W) *	-25 to +85	°C
T_{stor}	Storage temperature	-25 to +85	°C

Table 32: Absolute Maximum Ratings

7.2 Recommended Operating Conditions

Table 33 indicates the recommended operating conditions for Mars EB1 base board.

Symbol	Description	Rating	Unit
VCC_12V_IN	Supply voltage relative to GND	5 to 12	V
VCC_IO_[x]	VCC I/O input voltage relative to GND	Refer to the Mars module user manual	
$T_{ambient}$	Ambient temperature range for commercial boards (C) *	0 to +70	°C
	Ambient temperature range for wide range boards (W) *	-25 to +85	°C
T_{stor}	Storage temperature	-25 to +85	°C

Table 33: Recommended Operating Conditions

Warning!

** The components used on the hardware are specified for the relevant temperature range. The user must provide adequate cooling in order to keep the temperature of the components within the specified range.*

8 Ordering and Support

8.1 Ordering

Please use the Enclustra online request/order form for ordering or requesting information:
`http://www.enclustra.com/en/order/`

8.2 Support

Please follow the instructions on the Enclustra online support site:
`http://www.enclustra.com/en/support/`

List of Figures

List of Tables

References

[1] Enclustra General Business Conditions
http://www.enclustra.com/en/products/gbc/
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