Andromeda XZU90 Module

User Manual

Purpose

The purpose of this document is to present the characteristics of Andromeda XZU90 module to the user, and to provide the user with a comprehensive guide to understanding and using the Andromeda XZU90 module.

Summary

This document first gives an overview of the Andromeda XZU90 module followed by a detailed description of its features and configuration options. In addition, references to other useful documents are included.

Product Information	Code	Name
Product	AM-XZU90	Andromeda XZU90 Module

Document Information	Reference	Version	Date
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Approval Information	Name	Position	Date
Written by	WRUH	Design Engineer	28.02.2022
Verified by	ABUE, MKON	Design Expert	21.03.2022
Approved by	IJOS	Manager, BU SP	26.06.2023

Document History

Version	Date	Author	Comment
02	26.06.2023	MGOS	Improve consistency and readability. Fix typos.
01	21.03.2022	WRUH	Version 01

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1 Overview

1.1 General

1.1.1 Introduction

The Andromeda XZU90 module combines the Xilinx Zynq® UltraScale+ MPSoC (Multiprocessor System-on-Chip) device with fast DDR4 ECC SDRAM, eMMC flash, dual parallel quad SPI flash, dual Gigabit Ethernet PHY, USB 3.0 and thus forms a complete and powerful embedded processing system. This module is suitable for high-speed applications due to the high number of transceivers and due to the superior module connector performance.

The use of the Andromeda XZU90 module, in contrast to building a custom MPSoC hardware, significantly reduces development effort and redesign risk and improves time-to-market for the embedded system.

1.1.2 Warranty

Refer to the General Business Conditions, available on the Enclustra website [1].

> **Tip**
>
> The warranty of Enclustra modules is void if the FPGA's one-time programmable eFuses are blown. This operation is irreversible. Enclustra cannot test the module in case of a product return.

NOTICE

Data loss or unusable product

The fuses of the FPGA can be blown to activate the user-defined Advanced Encryption Standard (AES). After blowing the fuses, only content encrypted using a specific key can be loaded on the FPGA. Your key is unique and cannot be retrieved in case of loss.

- Keep your key in a secure location.

1.1.3 RoHS

The Andromeda XZU90 module is designed and produced according to the Restriction of Hazardous Substances (RoHS) Directive (2011/65/EC).

1.1.4 Disposal and WEEE

The Andromeda XZU90 module must be properly disposed of at the end of its life.

The Waste Electrical and Electronic Equipment (WEEE) Directive (2002/96/EC) is not applicable for the Andromeda XZU90 module.

1.1.5 Safety Recommendations and Warnings

Andromeda modules are not designed to be "ready for operation" for the end-user. These can only be used in combination with suitable base boards. Proper configuration of the hardware before usage is required.

Ensure that the power supply is disconnected from the board before inserting or removing the Andromeda XZU90 module, connecting interfaces, or connecting jumpers.

Touching the capacitors of the DC-DC converters can lead to voltage peaks and permanent damage; over-voltage on power or signal lines can also cause permanent damage to the module.

1.1.6 Electrostatic Discharge

Electronic boards are sensitive to electrostatic discharge (ESD). Ensure that the product is handled with care and only in an ESD-protected environment.

1.1.7 Electromagnetic Compatibility

The Andromeda XZU90 module is a Class A product (as defined in IEC 61000-3-2 standard) and is not intended for use in domestic environments. The product may cause electromagnetic interference, for which appropriate measures must be taken.

1.2 Features

- Xilinx Zynq® UltraScale+™ MPSoC
  - XCZU17EG/XCZU19EG device
  - FFVD1760 package
  - Quad-core ARM® Cortex™-A53 MPCore™ up to 1.333 GHz
  - Dual-core ARM® Cortex™-R5 MPCore™ up to 533 MHz
  - Mali-400 MP2 GPU
  - Xilinx 16nm FinFET+ FPGA fabric
- 686 user I/Os
  - 22 ARM peripheral I/Os (SPI, SDIO, CAN, I2C, UART)
  - 284 FPGA I/Os
    - 260 HP I/Os (1.0V - 1.8V)
    - 24 HD I/Os (1.8V - 3.3V)
  - 76 MGT channels
    - 28 GTY channels
      - Speedgrade 1 devices: 25.785 Gbit/s
      - Speedgrade 2 devices: 28.21 Gbit/s
    - 4 GTR chann
    - 44 GTH channels
      - Speedgrade 1 devices: 12.5 Gbit/s
      - Speedgrade 2 devices: 16.375 Gbit/s
    - 4 GTR channels @ 6 Gbit/s
  - 38 reference clock inputs
    - 14 GTY reference clock inputs
    - 22 GTH reference clock inputs
    - 2 GTR reference clock inputs
- Up to 5 × PCIe® Gen3 ×16 (Xilinx built-in PCIe integrated block using GTH/GTY lines)
- PCIe® Gen2 ×4 (Xilinx built-in PCIe hard block using GTR lines)
- 4 GB DDR4 ECC SDRAM on PS side
- 128 MB QSPI flash in dual parallel mode
- 16 GB eMMC flash
- 2 × Gigabit Ethernet (PS and PL)
- 1 × USB 2.0 (host/device)
- USB 3.0 (Xilinx built-in USB 3.0 hard block using GTR lines)
- Real-time clock
- CAN, UART, SPI, I2C, SDIO/MMC
- Small form factor 80 × 64 mm
- 12 V single supply

1.3 Deliverables

- Andromeda XZU90 module
- Andromeda XZU90 module documentation, available via download:
  - Andromeda XZU90 Module User Manual (this document)
  - Andromeda XZU90 Module Reference Design [2]
  - Andromeda XZU90 Module IO Net Length Excel Sheet [3]
  - Andromeda XZU90 Module FPGA Pinout Excel Sheet [4]
  - Andromeda XZU90 Module User Schematics (PDF) [5]
  - Andromeda XZU90 Module Known Issues and Changes [6]
  - Andromeda XZU90 Module Footprint (Altium) [7]
  - Andromeda XZU90 Module 3D Model (PDF) [8]
  - Andromeda XZU90 Module STEP 3D Model [9]
  - Andromeda Module Pin Connection Guidelines [10]
  - Andromeda Master Pinout [11]
  - Enclustra Build Environment [12] (Linux build environment; refer to Section 1.3.2 for details)
  - Enclustra Build Environment How-To Guide [13]
  - Petalinux BSP and Documentation [14]

1.3.1 Reference Design

The Andromeda XZU90 module reference design features an example configuration for the Zynq UltraScale+ MPSoC device, together with an example top level HDL file for the user logic.

A number of software applications are available for the reference design, that show how to initialize the peripheral controllers and how to access the external devices. Pre-compiled binaries are included in the archive, so that the user can easily check that the hardware is functional.

The reference design can be downloaded from Github: `https://github.com/enclustra`.

1.3.2 Enclustra Build Environment

The Enclustra Build Environment (EBE) [12] enables the user to quickly set up and run Linux on any Enclustra SoC module or system board. It allows the user to choose the desired target, and download all the required binaries, such as bitstream and FSBL. It downloads and compiles all required software, such as U-Boot, Linux, and BusyBox based root file system.

The Enclustra Build Environment features a graphical user interface (GUI) and a command line interface (CLI) that facilitates the automatic build flow.

The Enclustra Build Environment How-To Guide [13] describes in more detail how to use the EBE to customize the provided software for the user application. The document provides information on the configuration options for U-boot, Linux kernel and Buildroot, debugging possibilities for Linux applications, customization of device trees and integration of existing or new kernel drivers.

1.3.3 Petalinux BSP

The Enclustra Petalinux BSPs enable the user to quickly set up a Petalinux project and to run Linux on the Enclustra SoC module or system board.

The documentation [14] describes the build process in detail and allows a user without Petalinux knowledge to build and run the desired design on the target hardware.

1.4 Xilinx Tool Support

The MPSoC devices assembled on the Andromeda XZU90 module are supported by the Vivado HL Design Edition software for which a paid license is required. Contact Xilinx for further information.

2 Module Description

2.1 Block Diagram

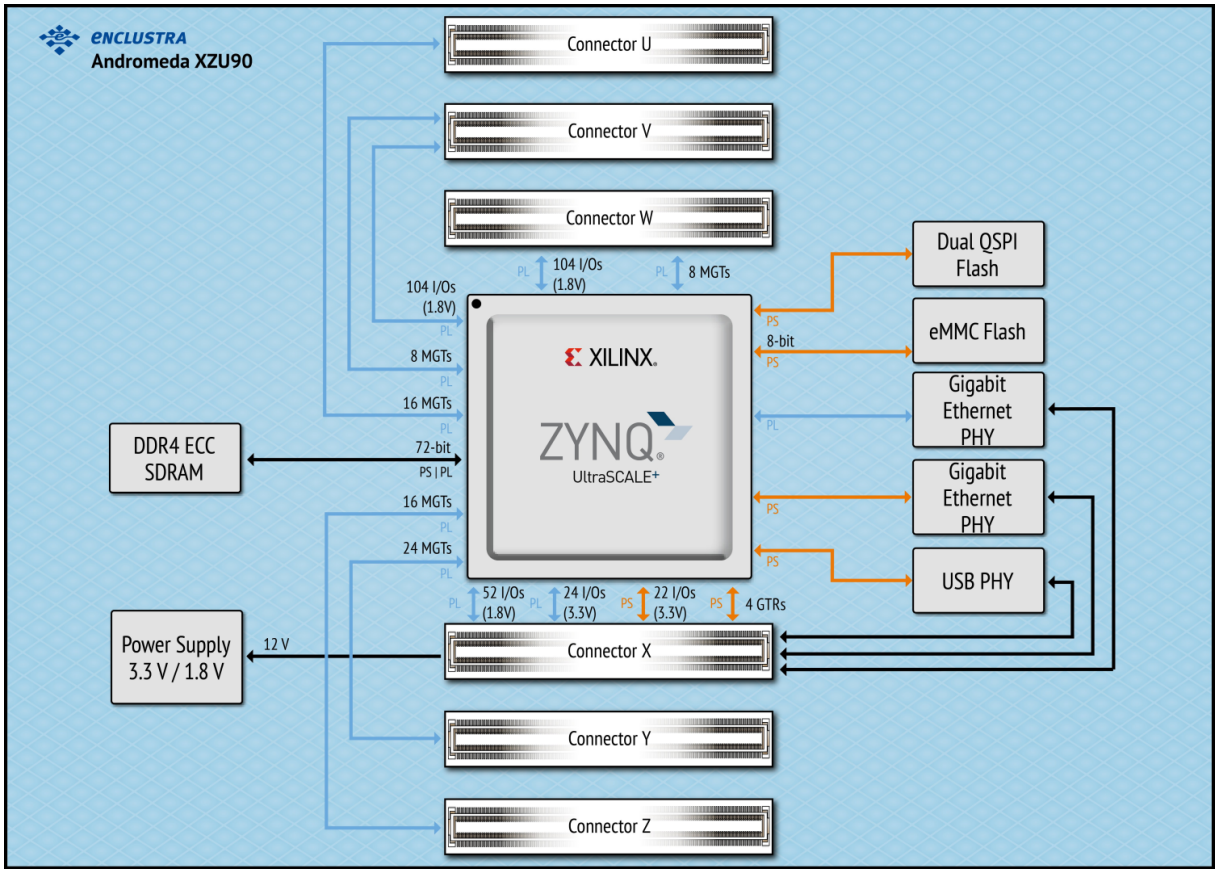

Figure 1: Hardware Block Diagram

The main component of the Andromeda XZU90 module is the Xilinx Zynq UltraScale+ MPSoC device. Most of its I/O pins are connected to the Andromeda module connector, making up to 686 regular user I/Os available to the user. Further, up to 76 MGT pairs are available on the module connector, making possible the implementation of several high-speed protocols such as 5 × PCIe Gen3 ×16, PCIe Gen2 ×4 and USB 3.0 (simultaneous usage of all the interfaces is limited to the available hardware resources i.e. number of transceivers and lane mapping).

The MPSoC device can boot from the on-board QSPI flash, from the eMMC flash or from an external SD card. For development purposes, a JTAG interface is connected to Andromeda module connector.

The available standard configurations include a 16 GB eMMC flash, a 128 MB quad SPI flash, 4 GB DDR4 SDRAM with ECC connected to the Processing System (PS).

Further, the module is equipped with two Gigabit Ethernet PHYs and one USB 2.0 PHY, making it ideal for communication applications.

A real-time clock is available on the Xilinx Zynq UltraScale+ MPSoC device.

On-board clock generation is based on a 33.333 MHz oscillator and two LVDS clocks: a 100 MHz and a 27 MHz oscillator providing reference clocks for the MGT GTR lines.

The module's internal supply voltages are generated from a single input supply of 12V DC. Most of these voltages can be monitored and measured via I2C. Some of the voltages are available on the Andromeda module connectors to supply circuits on the base board.

Six LEDs are connected to the MPSoC pins for status signaling.

2.2 Module Configuration and Product Models

Table 1 describes the available standard module configurations. The product model indicates the module type and main features. Figure 2 describes the fields within the product model. Custom configurations are available. Contact Enclustra for more information.

Product Model	MPSoC	DDR4 with ECC	Temperature
AM-XZU90-17EG-1E-D12E	XCZU17EG-1FFVD1760E	4 GB	0 to +85° C
AM-XZU90-19EG-2I-D12E	XCZU19EG-2FFVD1760I	4 GB	-40 to +85° C
AM-XZU90-19EG-2I-D13E	XCZU19EG-2FFVD1760I	8 GB	-40 to +85° C

Table 1: Standard Module Configurations

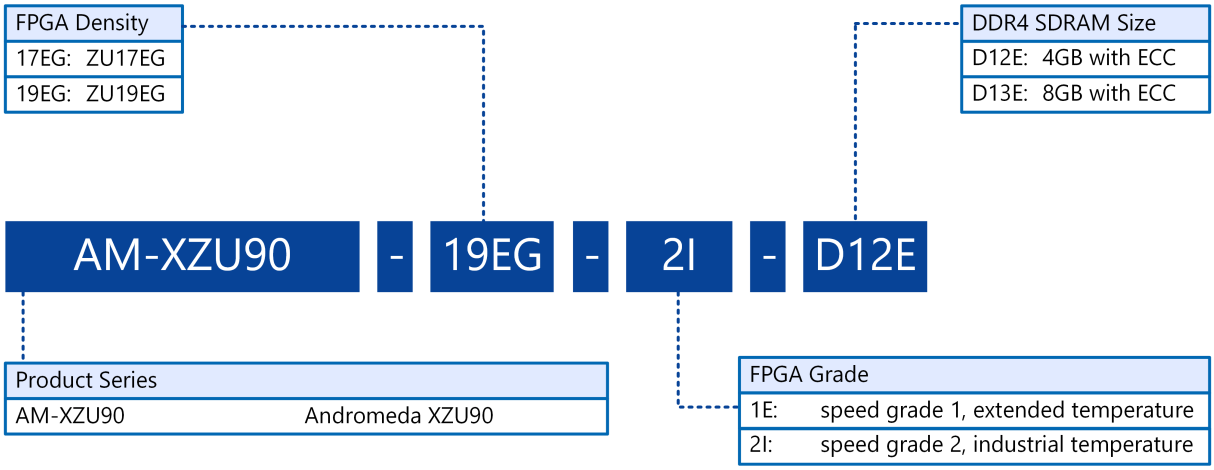

Figure 2: Product Model Fields

For the first revision modules or early access modules, the product model may not respect entirely this naming convention. Contact Enclustra for more information.

2.3 EN-Numbers and Product Models

Every product is uniquely labeled, showing the EN-number and serial number. An example is presented in Figure 3.

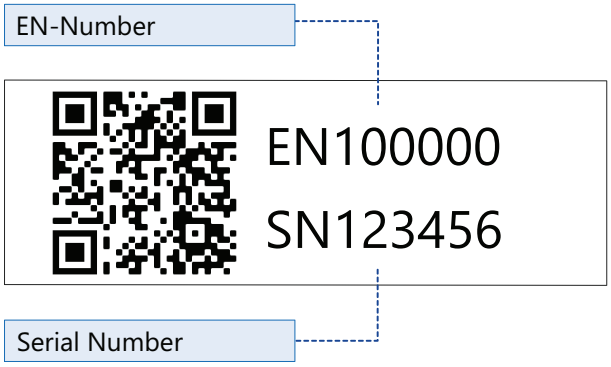

Figure 3: Module Label

The correspondence between EN-number and product model for each revision is shown in Table 2.

The known issues of the product and the changes between the revisions are described in the Andromeda XZU90 Module Known Issues and Changes document [6].

EN-Number	Product Model	Revision Number
EN102974	AM-XZU90-19EG-2I-D13E	R1.0
EN102975	AM-XZU90-17EG-1E-D12E	R1.0
EN104323	AM-XZU90-19EG-2I-D12E	R1.0

Table 2: EN-Numbers and Product Models

2.4 Top and Bottom Views

Depending on the hardware revision and configuration, the module may look slightly different than shown in this document.

2.4.1 Top View

Figure 4: Module Top View

2.4.2 Bottom View

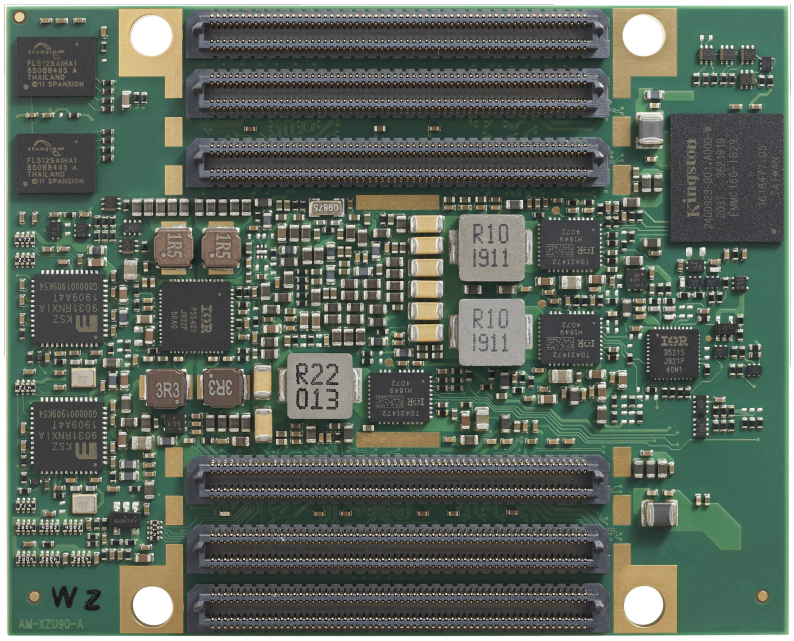

Figure 5: Module Bottom View

2.5 Top and Bottom Assembly Drawings

Depending on the hardware revision and configuration, the module may look slightly different than shown in this document.

2.5.1 Top Assembly Drawing

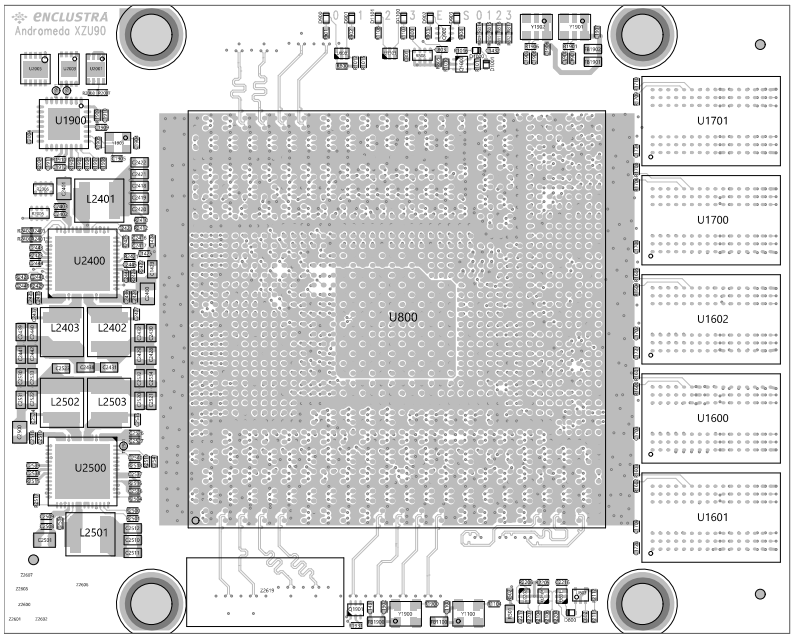

Figure 6: Module Top Assembly Drawing

2.5.2 Bottom Assembly Drawing

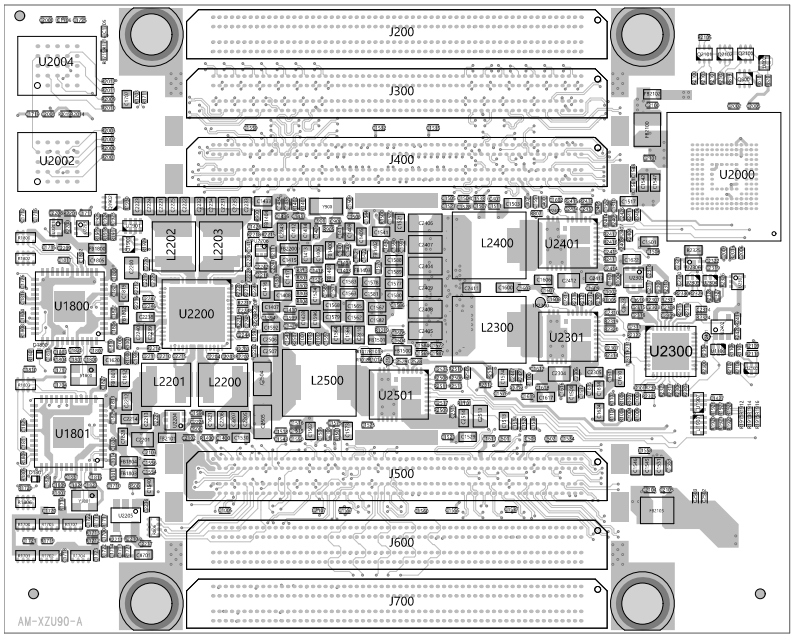

Figure 7: Module Bottom Assembly Drawing

2.6 Module Footprint and Mechanical Data

Figure 8 shows the dimensions of the module footprint on the base board.

The maximum component height under the module is dependent on the connector type - refer to Section 2.7 for detailed connector information.

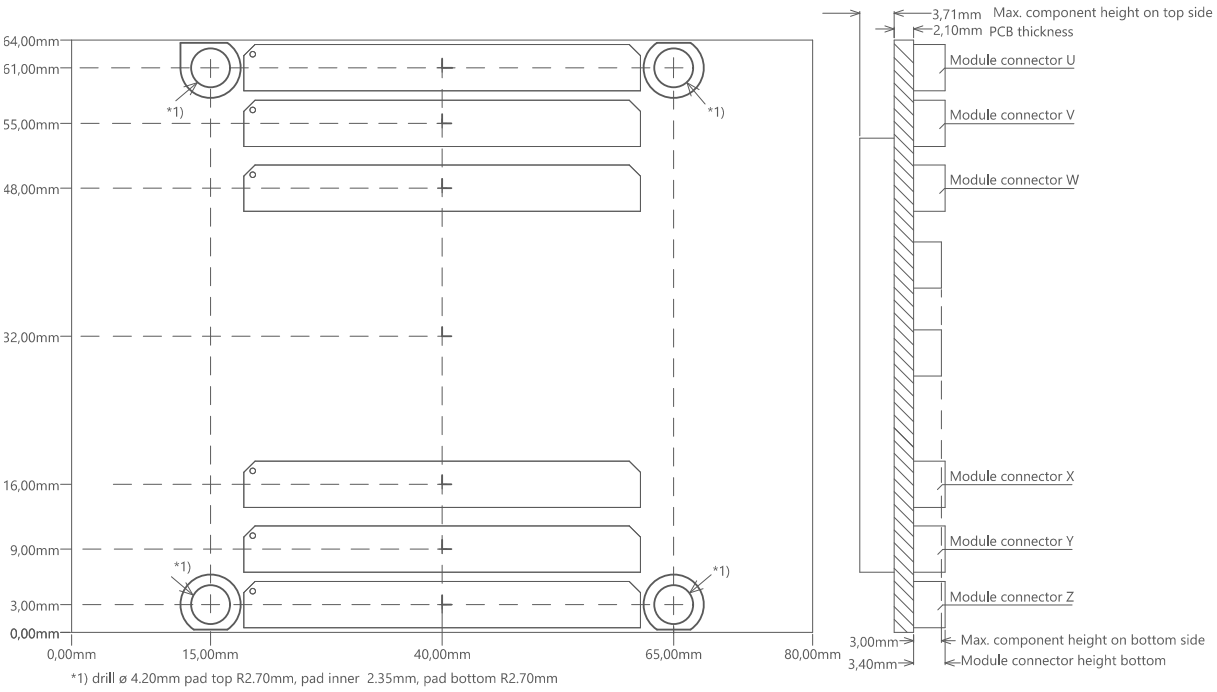

Figure 8: Module Footprint - Top View and Side View

Table 3 describes the mechanical characteristics of the Andromeda XZU90 module. A 3D model (PDF) and a STEP 3D model are available [8], [9].

Parameter	Value
Size	80 × 64 mm
Component height top	3.71 mm
Component height bottom	3 mm
Weight	66 g

Table 3: Mechanical Data

2.7 Module Connector

Six Samtec ADF6-60-03.5-L-4-2 240-pin 0.635 mm pitch headers with a total of 1440 pins have to be integrated on the base board. Four screw holes with a diameter of 4.2 mm are required to mechanically fasten the module to the base board. Do not use excessive force to tighten the screws, as this could damage the module.

The pinout of the module connector is found in the Andromeda Master Pinout Excel Sheet [11]. The module connector and its respective base board counter part are presented in Table 4. Refer to the connector datasheet for more information.

Reference	Type	Description
Andromeda module connector	ADM6-60-01.5-L-4-2	Samtec ADM6, 240-pin, 0.635 mm pitch
Base board connector	ADF6-60-03.5-L-4-2	Samtec ADM6, 240-pin, 0.635 mm pitch, 5 mm stacking height

Table 4: Module Connector Types

- Connector U: J200 A1-A60, B1-B60, C1-C60, D1-D60
- Connector V: J300 A1-A60, B1-B60, C1-C60, D1-D60
- Connector W: J400 A1-A60, B1-B60, C1-C60, D1-D60
- Connector X: J500 A1-A60, B1-B60, C1-C60, D1-D60
- Connector Y: J600 A1-A60, B1-B60, C1-C60, D1-D60
- Connector Z: J700 A1-A60, B1-B60, C1-C60, D1-D60

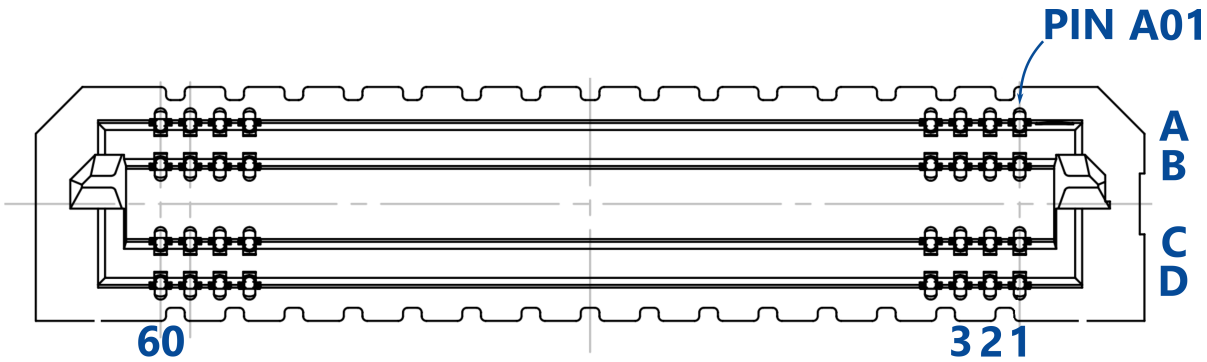

Figure 9: Pin Numbering for the Module Connector

NOTICE

Damage to the connectors

The connectors of the module and the base board can be damaged if the connectors are not properly aligned during installation.

- Align the connectors carefully before applying force on the module.
- Do not use excessive force to latch the module into the connectors on the base board.

NOTICE

Damage to the device when applying power

Depending on your base board, the Andromeda module could physically be mounted on the wrong connectors of the base board. The module and the base board can be damaged if the device is powered on while the wrong connectors are used.

- Ensure that the module connectors are attached to the corresponding base board connectors before powering on the device.

2.8 User I/O

2.8.1 Pinout

Information on the Andromeda XZU90 module pins can be found in the Enclustra Andromeda Master Pinout [11], and in the additional document Enclustra Module Pin Connection Guidelines [10].

Tip

The pin types on the schematic of the module connector and in the Master Pinout document are for reference only. On the Andromeda XZU90 module, the connected pins might not have the targeted functions (such as primary clocks, differential pins, MGT signals, etc).

Tip

The availability of certain pins might depend on the product model.

The naming convention for differential user I/Os is:
IO_B<BANK>_L<PAIR>_T<BYTE_GROUP>_<optional: SPECIAL_CLOCK_FUNCTION>_<POLARITY>.

For example, IO_B66_L9_T1_P belongs to pair 9 and byte group 1 of I/O bank 66. It has positive polarity when used in a differential pair.

Global clock capable pins are additionaly marked with “GC” (HP I/O banks) or with “HDGC” (HD I/O banks) in their name at the <optional: SPECIAL_CLOCK_FUNCTION> position. Quad byte clock and dedicated byte clock capable pins are marked with “QBC” or “DBC” in their name at the <optional: SPECIAL_CLOCK_FUNCTION> position.

The naming convention for single-ended user I/Os is:
IO_B<BANK>_DS_T<BYTE_GROUP>_<optional: SPECIAL_FUNCTION>_<POLARITY>.

For example, IO_B66_DS_T1 is single-ended and belongs to byte group 1 of I/O bank 66.

There are four single-ended pins on each HP bank. One of those four single-ended pins is additionally marked with “VRP”. This pin can be used to connect a reference resistor if DCI (digitally controlled impedance) standards are used in the respective bank. Otherwise it can be used as an I/O pin. For details, refer to the Xilinx documentation.

Table 5 includes information related to the total number of I/Os available in each I/O bank and possible limitations.

Signal Name	Signals	Pairs	Differential	Single-ended	Bank	Bank Type[1]
IO_B65_<...>	52	24	In/Out	In/Out	65	HP
IO_B66_<...>	52	24	In/Out	In/Out	66	HP
IO_B69_<...>	52	24	In/Out	In/Out	69	HP
IO_B70_<...>	52	24	In/Out	In/Out	70	HP
IO_B71_<...>	52	24	In/Out	In/Out	71	HP
IO_B91_<...>	24	12	In/Out (no LVDS/LVPECL outputs supported; internal differential termination not supported) Refer to Section 2.8.3 for details.	In/Out	91	HD
Total	**284**	**132**	-	-	-	-

Table 5: User I/Os

The multi-gigabit transceiver (MGT) are described in section 2.9.

2.8.2 I/O Pin Exceptions

The I/O pin exceptions are pins with special functions or restrictions (for example, when used in combination with certain Andromeda boards they may have a specific role).

PCIe Reset Signal (PERST#)

Table 6 lists the I/O pin exceptions on the Andromeda XZU90 module related to the PCIe reset connection.

I/O Name	Module Connector Pin	Description
PS_MIO32_PERSTPL#_LED1#	X-B52	When the pin has a low value, IO_B65_DS_T3_PERST# pin (module connector pin V-B42, dedicated FPGA pin for PL PCIe PERST# implementation) is pulled to ground via a level shifter
PS_MIO33_PERSTPS#_LED0#	X-B51	This pin is connected to MIO33 for PS PCIe PERST# implementation

Table 6: I/O Pin Exceptions - PERST#

Pins PS_MIO33_PERSTPS#_LED0# and PS_MIO32_PERSTPL#_LED1# are also connected to two LEDs on the module.

In situations in which PCIe functionality is not required, PS_MIO33_PERSTPS#_LED0#, PS_MIO32_PERSTPL#_LED1# and IO_B65_DS_T3_PERST# pins can be used for other functions.

[1] HD = high density pins, HP = high performance pins; Refer to the Zynq UltraScale+ MPSoC Overview [19] for details.

2.8.3 Differential I/Os

When using differential pairs, a differential impedance of 100 Ω must be matched on the base board, and the two nets of a differential pair must have the same length.

The information regarding the length of the signal lines from the MPSoC device to the module connector is available in Andromeda XZU90 Module IO Net Length Excel Sheet [3]. This enables the user to match the total length of the differential pairs on the base board if required by the application.

> **Tip**
>
> The trace length of various signals may change between revisions of the Andromeda XZU90 module. Use the information provided in the Andromeda XZU90 Module IO Net Length Excel Sheet [3] to check which signals are affected. The differential signals will also be routed differentially in subsequent product revisions.

The I/Os in the HD bank 91 can be used only as differential inputs when LVDS/LVPECL standards are used; LVDS/LVPECL outputs are not supported.

Internal differential termination is not supported for the HD pins; differential input pairs on the module connector may be terminated by external termination resistors on the base board (close to the module pins).

2.8.4 I/O Banks

Table 7 describes the main attributes of the Programmable Logic (PL) and Processing System (PS) I/O banks, and indicates which peripherals are connected to each I/O bank. All I/O pins within a particular I/O bank must use the same I/O (V_IO) and reference (VREF) voltages.

Bank	Bank Type	Connectivity	V_IO	VREF
224	GTH	Module connector	0.9 V	-
225	GTH	Module connector	0.9 V	-
226	GTH	Module connector	0.9 V	-
227	GTH	Module connector	0.9 V	-
228	GTH	Module connector	0.9 V	-
229	GTH	Module connector	0.9 V	-
230	GTH	Module connector	0.9 V	-
231	GTH	Module connector	0.9 V	-
232	GTH	Module connector	0.9 V	-
233	GTH	Module connector	0.9 V	-
234	GTH	Module connector	0.9 V	-
128	GTY	Module connector	0.9 V	-
129	GTY	Module connector	0.9 V	-
130	GTY	Module connector	0.9 V	-

Continued on next page...

Bank	Bank Type	Connectivity	V_IO	VREF
131	GTY	Module connector	0.9 V	-
132	GTY	Module connector	0.9 V	-
133	GTY	Module connector	0.9 V	-
134	GTY	Module connector	0.9 V	-
65	HP	Module connector	User selectable V_IO_B65	User selectable 0.5 × V_IO_B65
66	HP	Module connector	User selectable V_IO_B66	User selectable 0.5 × V_IO_B66
69	HP	Module connector	User selectable V_IO_B69	User selectable 0.5 × V_IO_B69
70	HP	Module connector	User selectable V_IO_B70	User selectable 0.5 × V_IO_B70
71	HP	Module connector	User selectable V_IO_B71	User selectable 0.5 × V_IO_B71
90	HD	Gigabit Ethernet PHY 1, I2C, LEDs, PL_RST, power converters	1.8 V	-
91	HD	Module connector	User selectable V_IO_B91	-
503	PS CONFIG	FPGA PS Configuration	User selectable V_IO_CFG	-
504	PS DDR	DDR4 SDRAM	1.2 V	-
500	PS MIO	eMMC and QSPI flash devices, I2C	1.8 V	-
501	PS MIO	UART 0, UART 1, I2C, LEDs, SD card, DP AUX, module connector	User selectable V_IO_CFG	-
502	PS MIO	USB PHY 0, Gigabit Ethernet PHY 0	1.8 V	-
505	PS GTR	Module connector	0.85 V	-

Table 7: I/O Banks

2.8.5 V_IO Usage

The VCCO voltages for the I/O banks located on the module connector are configurable by applying the required voltage to the V_IO_B[x], respectively V_IO_CFG pins. All V_IO_B[x] or V_IO_CFG pins of the same bank must be connected to the same voltage.

For compatibility with other Enclustra Andromeda modules, it is recommended to use a single I/O voltage per module connector.

Signal Name	MPSoC Pins	Supported Voltages	Module Connector Pins
V_IO_CFG	VCCO_PSIO1_501, VCCO_PSIO3_503	1.8V - 3.3V ±5%	X-C52
V_IO_B65	VCCO_65	1.0V - 1.8V ±5%	V-D43, V-D57
V_IO_B66	VCCO_66	1.0V - 1.8V ±5%	V-D3, V-D17
V_IO_B69	VCCO_69	1.0V - 1.8V ±5%	W-D3, W-D17
V_IO_B70	VCCO_70	1.0V - 1.8V ±5%	W-D43, W-D57
V_IO_B71	VCCO_71	1.0V - 1.8V ±5%	X-A3, X-A17
V_IO_B91	VCCO_91	1.8V - 3.3V ±5%[2]	X-B35

Table 8: V_IO Pins

Figure 10 illustrates the requirements of the V_IO power sequence. Do not power the V_IO pins when PWR_GOOD and PWR_EN signals are not active. If the module is not powered, make sure that the V_IO voltages are disabled, for example, by using a switch that uses PWR_GOOD as enable signal on the base board.

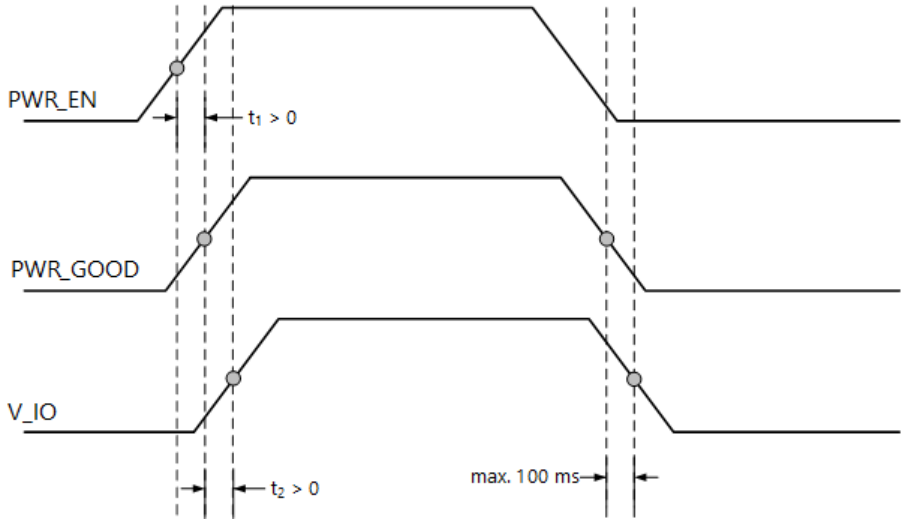

Figure 10: Power Sequence - V_IO in Relation with PWR_GOOD and PWR_EN Signals

[2] For voltages of 3.3 V for V_IO_B91 the tolerance range is -5% to +3%.

NOTICE

Damage to the device due to unsuitable voltage

Unsuitable voltages may damage the MPSoC device as well as other devices on the Andromeda XZU90 module.

- Only use V_IO voltages compliant with the assembled MPSoC device.

NOTICE

Damage to the device due to floating V_IO pins

Floating V_IO pins reduce ESD protection.

- Do not leave any V_IO pin floating.

⚠ CAUTION

Injury due to uncontrolled device

If an I/O is connected to an external device, violating the power sequence or leaving the corresponding V_IO pin floating will leave the pin in an undefined state. This can lead to any behavior of the devices attached to this pin and, potentially, to damage or injuries.

- Follow the power sequence diagram shown in Figure 10. This ensures that the I/Os are tri-stated at power-on and power-off.
- Do not leave V_IO pins floating.

2.8.6 Signal Terminations

Differential Inputs

Internal differential termination is not supported for the HD pins. Differential input pairs on the module connector may be terminated by external termination resistors on the base board (close to the module pins).

Single-Ended Outputs

There are no series termination resistors on the Andromeda XZU90 module for single-ended outputs. If required, series termination resistors may be assembled on the base board (close to the module pins).

2.8.7 Multiplexed I/O (MIO) Pins

Details on the MIO/EMIO terminology are available in the Zynq UltraScale+ MPSoC Technical Reference Manual [15].

Some of the MIO pins on the Andromeda XZU90 module are connected to on-board peripherals, while others are available as GPIOs; the suggested functions below are for reference only - always verify your MIO pinout with the Xilinx device handbook.

Table 9 gives an overview over the MIO pin connections on the Andromeda XZU90 module. Only the pins marked with “user functionality” are available on the module connector.

MIO Pins	Default Function	Connection
0-5	QSPI0 flash	QSPI0 flash
6	QSPI feedback clock	-
7-12	QSPI1 flash	QSPI1 flash
13-22	eMMC flash	eMMC flash
23-25	User I2C	Module connector, can optionally be connected to PL buck converters (not default)
26 27	UART0 RX[3]/user functionality UART0 TX[3]/user functionality	Module connector
28 29	UART1 RX[3]/user functionality UART1 TX[3]/user functionality	Module connector
30, 31, 38	Management (MGMT) I2C	Module connector; I2C bus connected by default to PL buck converters, PS buck converter, to optional user FRAM, secure EEPROM, ETH PHY 0 interrupt
32-33	PCIe PERST# signals for PS and PL[4]	Module connector, LEDs
34-37	DisplayPort AUX/user functionality	Module connector
43	PS peripheral reset	Reset signal for Ethernet PHY 0, Ethernet PHY 1, USB PHY 0, eMMC, QSPI flash devices, secure EEPROM
39-51	SD card/user functionality	Module connector
52-63	USB 0	USB 2.0 PHY 0
64-77	Ethernet 0	Ethernet PHY 0

Table 9: MIO Pins Connections Overview

2.8.8 Analog Inputs

The Zynq UltraScale+ MPSoC devices contain a system monitor in the PL and an additional system monitor block in the PS. These are used to sample analog inputs and to collect information on the internal voltages and temperatures.

The system monitor block in the PL provides a 10-bit ADC, which supports up to 17 external analog lines (1 dedicated differential input, 16 auxiliary differential inputs). The auxiliary analog lines of the MPSoC device are available on the module connector; these are the differential pins on the HD and HP banks having the text "AD" in the FPGA symbol in the schematics. The ADC lines are always used differentially; for single-ended applications, the *_N line must be connected to GND.

[3] UART RX is an MPSoC input; UART TX is an MPSoC output.
[4] Used for PCIe PERST# connection implementation. Refer to Section 2.8.2 for details.

The analog input signals can be connected to any normal I/O FPGA bank, provided that all analog pins belong to the same bank. Note that the HD I/O banks have a limited number of analog inputs and they must be connected directly to the SYSMONE4 primitive instead of to the Xilinx System Management Wizard IP core.

The dedicated channel is available on the module connector on pins X-D56 and X-D57 and can be used for thermal monitoring.

For detailed information on the ADC and system monitor, refer to the UltraScale Architecture System Monitor document [16], Zynq UltraScale+ MPSoC Technical Reference Manual [15] and System Management Wizard Product Guide [18].

Table 10 presents the ADC Parameters for the PL System Monitor. The PS System Monitor is only used for monitoring the on-chip power supply voltages and die temperature.

Parameter	Value (PL Sysmon)
VCC_ADC	1.8 V
VREF_ADC	Internal
ADC Range	0-1 V
Sampling Rate per ADC	0.2 MSPS
Total number of channels available on the module connector	17 (auxiliary inputs and dedicated channel)

Table 10: System Monitor (PL) Parameters

2.9 Multi-Gigabit Transceiver (MGT)

There are three types of multi-gigabit transceivers available on the Andromeda XZU90 module: GTY transceivers (connected to the PL), GTH transceivers (connected to the PL) and GTR transceivers (connected to the PS).

MGT Type	Speed Grade 1 Performance [Gbit/s]	Speed Grade 2 Performance [Gbit/s]
GTY	25.785	28.21
GTH	12.5	16.375
GTR	6	6

Table 11: MGT Speed Grade and Performance Overview

Note that Samtec module connector has a performance limit of 25 Gbit/s for NRZ encoding.

> **Tip**
>
> The maximum data rate on the MGT lines on the Andromeda XZU90 module depends on the routing path for these signals. When using MGTs at high performance rates, ensure adequate signal integrity over the full signal path.

NOTICE

Damage to the MGT lines

No AC coupling capacitors are placed on the Andromeda XZU90 module on the MGT lines.

- If required by your application, ensure that capacitors are mounted on the base board, close to the module pins.

GTY Transceivers

There are 28 GTY MGTs available on the Andromeda XZU90 module organized in 7 FPGA banks - Table 12 describes the connections.

The naming convention for the GTY MGT I/Os is:
MGT_B<BANK>_<FUNCTION>_<POLARITY>.

For example, MGT_B128_TX2_N is a transmit pin with negative polarity located on MGT I/O bank 128.

Signal Name	Signal Description	Pairs	I/O Bank
MGT_B128_RX<...>	MGT receivers	4	128
MGT_B128_TX<...>	MGT transmitters	4	
MGT_B128_REFCLK<...>	MGT reference input clocks	2	
MGT_B129_RX<...>	MGT receivers	4	129
MGT_B129_TX<...>	MGT transmitters	4	
MGT_B129_REFCLK<...>	MGT reference input clocks	2	
MGT_B130_RX<...>	MGT receivers	4	130
MGT_B130_TX<...>	MGT transmitters	4	
MGT_B130_REFCLK<...>	MGT reference input clocks	2	
MGT_B131_RX<...>	MGT receivers	4	131
MGT_B131_TX<...>	MGT transmitters	4	
MGT_B131_REFCLK<...>	MGT reference input clocks	2	
MGT_B132_RX<...>	MGT receivers	4	132
MGT_B132_TX<...>	MGT transmitters	4	
MGT_B132_REFCLK<...>	MGT reference input clocks	2	
MGT_B133_RX<...>	MGT receivers	4	133
MGT_B133_TX<...>	MGT transmitters	4	
MGT_B133_REFCLK<...>	MGT reference input clocks	2	
MGT_B134_RX<...>	MGT receivers	4	134

Continued on next page...

Signal Name	Signal Description	Pairs	I/O Bank
MGT_B134_TX<...>	MGT transmitters	4	
MGT_B134_REFCLK<...>	MGT reference input clocks	2	

Table 12: MGT GTY Pairs

12 of the GTY pairs and six corresponding clocks are routed to module connector U, while eight GTY pairs and four reference input clock differential pairs are routed to module connector V. Furthermore, eight GTY pairs and four corresponding clocks are routed to module connector W.

GTH Transceivers

There are 44 GTH MGTs available on the Andromeda XZU90 module organized in 11 FPGA banks - Table 13 describes the connections.

The naming convention for the GTH MGT I/Os is:
MGT_B<BANK>_<FUNCTION>_<POLARITY>.

For example, MGT_B228_TX2_N is a transmit pin with negative polarity located on MGT I/O bank 228.

Signal Name	Signal Description	Pairs	I/O Bank
MGT_B224_RX<...>	MGT receivers	4	224
MGT_B224_TX<...>	MGT transmitters	4	
MGT_B224_REFCLK<...>	MGT reference input clocks	2	
MGT_B225_RX<...>	MGT receivers	4	225
MGT_B225_TX<...>	MGT transmitters	4	
MGT_B225_REFCLK<...>	MGT reference input clocks	2	
MGT_B226_RX<...>	MGT receivers	4	226
MGT_B226_TX<...>	MGT transmitters	4	
MGT_B226_REFCLK<...>	MGT reference input clocks	2	
MGT_B227_RX<...>	MGT receivers	4	227
MGT_B227_TX<...>	MGT transmitters	4	
MGT_B227_REFCLK<...>	MGT reference input clocks	2	
MGT_B228_RX<...>	MGT receivers	4	228
MGT_B228_TX<...>	MGT transmitters	4	
MGT_B228_REFCLK<...>	MGT reference input clocks	2	
MGT_B229_RX<...>	MGT receivers	4	229
MGT_B229_TX<...>	MGT transmitters	4	
MGT_B229_REFCLK<...>	MGT reference input clocks	2	

Continued on next page...

Signal Name	Signal Description	Pairs	I/O Bank
MGT_B230_RX<...>	MGT receivers	4	230
MGT_B230_TX<...>	MGT transmitters	4	
MGT_B230_REFCLK<...>	MGT reference input clocks	2	
MGT_B231_RX<...>	MGT receivers	4	231
MGT_B231_TX<...>	MGT transmitters	4	
MGT_B231_REFCLK<...>	MGT reference input clocks	2	
MGT_B232_RX<...>	MGT receivers	4	232
MGT_B232_TX<...>	MGT transmitters	4	
MGT_B232_REFCLK<...>	MGT reference input clocks	2	
MGT_B233_RX<...>	MGT receivers	4	233
MGT_B233_TX<...>	MGT transmitters	4	
MGT_B233_REFCLK<...>	MGT reference input clocks	2	
MGT_B234_RX<...>	MGT receivers	4	234
MGT_B234_TX<...>	MGT transmitters	4	
MGT_B234_REFCLK<...>	MGT reference input clocks	2	

Table 13: MGT GTH Pairs

24 of the GTH pairs and 12 corresponding clocks are routed to module connector Y, while 16 GTH pairs and eight reference input clock differential pairs are routed to module connector Z. Furthermore, four GTH pairs and two corresponding clocks are routed to module connector U.

GTR Transceivers

There are four GTR MGT pairs and two reference input clock differential pairs on the Andromeda XZU90 module connected to I/O bank 505; these are routed to module connector X.

The naming convention for the GTR MGT I/Os is:
MGT_B<BANK>_<FUNCTION>_<POLARITY>.

For example, MGT_B505_RX1_N is a receive pin with negative polarity and is located on PS GTR bank (bank 505).

All Andromeda XZU90 module variants support the implementation of a PCIe Gen2 ×4 interface.

The GTR pairs support data rates of up to 6 Gbit/s and can be used for the implementation of several interfaces such as PCIe Gen2 ×4, USB 3.0, DisplayPort, SATA, or Ethernet SGMII. Refer to the Zynq UltraScale+ MPSoC Technical Reference Manual [15] and to the Zynq UltraScale+ MPSoC Overview [19] for details.

A 100 MHz LVDS oscillator and a 27 MHz CMOS oscillator provide reference clock inputs to the PS GTR bank 505. Refer to Section 2.11 for details.

2.10 Power

2.10.1 Power Generation Overview

The Andromeda XZU90 module uses several 12 V DC power inputs for generating the on-board supply voltages for the PS and PL supplies of the MPSoC. Some of the PL voltages (1.8 V, 3.3 V) are accessible on the module connector.

Table 14 lists the PS power supplies generated on the module.

Output Supply Name	Voltage Value	Rated Current	Input Supply Name	Shut down via PWR_EN	Influences PWR_GOOD
V_PSINT	0.85 V (PS core supply and GTR transceiver supply)	4 A	V_MOD_PS	Yes	Yes
V_3V3_PS	3.3 V	2 A	V_MOD_PS	No	Yes
V_1V8_PS	1.8 V	2 A	V_MOD_PS	Yes	Yes
V_1V2_PS	1.2 V	4 A	V_MOD_PS	Yes	Yes
V_VTT_PS	0.6 V (DDR termination)	0.5 A	V_1V2_PS	Yes	Yes
V_5V_PS	5 V	0.3 A	V_MOD_PS	No	No
V_2V5_PS	2.5 V	0.3 A	V_3V3_PS	Yes	No

Table 14: Generated PS Power Supplies

Table 15 lists the PL power supplies generated on the module.

Output Supply Name	Voltage Value	Rated Current	Input Supply Name	Shut down via PWR_EN	Influences PWR_GOOD
V_INT	0.85 V (PL core supply)	30 A	V_MOD_PL_W	Yes	Yes
V_5V_PL	5 V	0.3 A	V_MOD_PL_W	No	No
V_3V3_PL	3.3 V	2 A	V_MOD_PL_W	No	Yes
V_INT_IO	0.85 V	4 A	V_MOD_PL_W	Yes	Yes
V_1V8_PL	1.8 V	4 A	V_MOD_PL_W	Yes	Yes
V_1V2_MGT	1.2 V	22 A	V_MOD_PL_X	Yes	Yes
V_1V8_MGT	1.8 V	2 A	V_MOD_PL_X	Yes	Yes
V_0V9_MGT	0.9 V	8 A	V_MOD_PL_X	Yes	Yes

Table 15: Generated PL Power Supplies

On the standard product models, the PS and PL core supplies are set to 0.85 V. For custom models, in which different speedgrades are used, the DC/DC converters can be configured to generate the required voltages for MPSoC as specified in the Xilinx documentation.

Refer to the Enclustra Module Pin Connection Guidelines for general rules on the power pins [10].

Power Converter Synchronization

Some switching converters used on the Andromeda XZU90 module support synchronization of the switching frequency with an external clock. The module includes a power synchronization circuit, which may drive a clock generated by the MPSoC device to these DC/DC converters.

The converters which can be synchronized are responsible for the generation of the following voltages:

- V_3V3_PS
- V_1V8_PS
- V_1V2_PS
- V_VTT_PS
- V_3V3_PL
- V_INT
- V_INT_IO
- V_1V8_PL
- V_1V8_MGT
- V_1V2_MGT
- V_0V9_MGT

The synchronization clock signal PWR_SYNC can be generated by the MPSoC device and is located on HD Bank 90 on the IO_L2P_AD10P_90 pin (package pin R14).

The synchronization frequency valid for all switching DC/DC converters on-board and compensation networks must lie in the range 200..1000 kHz.

The sync clock must be within ± 6.25% of the programmed converter frequency to ensure the converter will lock on phase and frequency.

2.10.2 Power Enable/Power Good

The Andromeda XZU90 module provides two power enable inputs on the module connector. These inputs may be used to shut down PS and PL DC/DC converters. The list of regulators that can be disabled via PWR_EN signals is provided in Section 2.10.1.

There are two sets of PWR_EN and PWR_GOOD signals for PS and PL sides. This allows the user to control and monitor the PS and PL supplies separately. By default, PWR_EN_PL is generated from PWR_EN signal (acting as a global enable signal), and PWR_GOOD reflects the general power good status for both PS and PL sides. The signals are pulled to V_3V3_PL/PS on the Andromeda XZU90 module with a 4.7 kΩ resistor.

The PWR_GOOD signals are open collector signals and must not be used to drive a load directly. These signals are pulled to GND if the on-board regulators fail or if the module is disabled via PWR_EN. The list of regulators that influence the state of PWR_GOOD signals is provided in Section 2.10.1.

Pin Name	Module Connector Pin	Remarks
PWR_EN	X-D58	Floating/3.3 V: Module (PS) power enabled Driven low: Module (PS) power disabled
PWR_GOOD	X-D59	0 V: Module (PS) supply not ok 3.3 V: Module (PS) supply ok
PWR_EN_PL	X-C32	Floating/3.3 V: Module (PL) power enabled Driven low: Module (PL) power disabled
PWR_GOOD_PL	X-C33	0 V: Module (PL) supply not ok 3.3 V: Module (PL) supply ok

Table 16: Module Power Status and Control Pins

NOTICE

Damage to the device due to unsuitable voltage

Appling unsuitable voltage to the PWR_EN pins can damage the Andromeda XZU90 module.

- Do not apply any other voltages to the PWR_EN pins than 3.3 V or GND.
- PWR_EN pins can be left unconnected.

⚠ CAUTION

Injury due to uncontrolled device

If an I/O is connected to an external device, violating the power sequence or leaving the corresponding V_IO pin floating will leave the pin in an undefined state. This can lead to any behavior of the devices attached to this pin and, potentially, to damage or injuries.

- Follow the power sequence diagram shown in Figure 10. This ensures that the I/Os are tri-stated at power-on and power-off.
- Do not leave V_IO pins floating.

2.10.3 Voltage Supply Inputs

Table 17 describes the power supply inputs on the Andromeda XZU90 module. The voltages used as supplies for the I/O banks are described in Section 2.8.5.

Supply Name	Module Connector Pins	Voltage	Description
V_MOD_PS	X-B60, X-D60	12 V ±5%	Supply for PS voltage regulators - see Table 14 for details. The input current is rated at 0.66 A (0.33 A per connector pin).
V_MOD_PL_X	X-C5, X-C11, X-C17, X-D7, X-D15	12 V ±5%	Supply for PL voltage regulators - see Table 15 for details. The input current is rated at 1.65 A (0.33 A per connector pin).
V_MOD_PL_W	W-A7, W-A15, W-A47, W-A55, W-B5, W-B11, W-B17, W-B45, W-B51, W-B57	12 V ±5%	Supply for PL voltage regulators - see Table 15 for details. The input current is rated at 3.3 A (0.33 A per connector pin).
VCC_BAT	X-A59	1.2 - 1.5 V	Battery voltage for MPSoC battery-backed RAM and battery-backed RTC

Table 17: Voltage Supply Inputs

2.10.4 Voltage Supply Outputs

Table 18 presents the supply voltages generated on the Andromeda XZU90 module that are available on the module connector.

Supply Name	Module Connector Pins	Voltage	Maximum Current[5]	Comment
V_3V3_PS	X-B59	3.3 V ±5%	0.33 A	Always active
V_3V3_PL	W-D11, X-A11	3.3 V ±5%	0.33 A	Always active
V_1V8_PL	W-C7, W-C15, X-B7, X-B15	1.8 V ±5%	1.32 A (0.33 A per pin)	Controlled by PWR_EN

Table 18: Voltage Supply Outputs

NOTICE

Damage to the device due to unsuitable usage of the output pins

- Do not connect any power supply to the voltage supply outputs.
- Do not short circuit any of the voltage supply outputs to GND.

[5] The maximum available output current depends on your design. See sections 2.10.1 and 2.10.5 for details.

2.10.5 Power Consumption

The power consumption of any MPSoC device strongly depends on the application (on the configured bitstream and I/O activity).

To estimate the power consumption of your design, use the Xilinx Power Estimator available on the Xilinx website.

2.10.6 Heat Dissipation

High performance devices like the Xilinx Zynq UltraScale+ MPSoC need cooling in most applications; always make sure the MPSoC is adequately cooled.

A third-party heat sink body (ATS) and an additional gap pad (t-Global) may be used. Table 19 lists the heat sink and thermal pad part numbers that are compatible with the Andromeda XZU90 module.

Product Name	Package Name	ATS Heat Sink	t-Global Thermal Pad
Andromeda XZU90	FFVC1156 [20]	ATS-52425P-C1-R0	TG-A6200-40-40-1.0

Table 19: Heat Sink Type

Tip

The adhesive heat sink part is recommended only for prototyping purposes. When the module is used in environments subject to vibrations, additional mechanical fixation is recommended.

NOTICE

Damage to the device due to overheating

Depending on the user application, the Andromeda XZU90 module may consume more power than can be dissipated without additional cooling measures.

- Ensure that the MPSoC is always adequately cooled by installing a heat sink and/or providing air flow.

2.10.7 Voltage Monitoring

Two pins on the module connector on the Andromeda XZU90 module are marked as VMON. These are voltage monitoring outputs that are used in the production test for measuring some of the on-board voltages.

It is not allowed to draw power from the voltage monitoring outputs.

Several other voltages generated on the module can be monitored via I2C.

Table 20 presents the VMON pins on the Andromeda XZU90 module.

Pin Name	Module Connector XPin	Connection	Description
PWR_VMON_XA39	X-A39	V_0V85_GTR	GTR transceiver supply
PWR_VMON_XC39	X-C39	V_2V5_PS	2.5 V PS supply

Table 20: Voltage Monitoring Outputs

> **Tip**
>
> The voltage monitoring outputs are for Enclustra-use only. Pinout changes may be applied between revisions.

2.11 Clock Generation

A 33.333 MHz oscillator is used for the Andromeda XZU90 module clock generation; the 33.333 MHz clock is fed to the PS. For the PL side, an additional 33.333 MHz oscillator is connected to HD bank 90.

A 100 MHz LVDS oscillator and a 27 MHz CMOS oscillator provide reference clock inputs to the PS GTR bank 505. A 24 MHz clock and a 25 MHz clock are used for the USB PHYs and Ethernet PHYs respectively. The crystal pads for the MPSoC RTC are connected to a 32.768 kHz oscillator on the Andromeda XZU90 module.

Table 21 describes the clock connections to the MPSoC device.

Signal Name	Frequency	Package Pin	MPSoC Pin Type
CLK33_PS	33.333 MHz	AA29	PS_REF_CLK
CLK33_PL	33.333 MHz	K13	IO_L8P_HDGC_AD4P_90
CLK27_P	27 MHz	AK33	PS_MGTREFCLK3P_505
CLK27_N		AK34	PS_MGTREFCLK3N_505
CLK100_P	100 MHz	AL31	PS_MGTREFCLK2P_505
CLK100_N		AL32	PS_MGTREFCLK2N_505
PS_PADI	32.768 kHz	AD30	PS_PADI (crystal pad input for MPSoC built-in RTC)
PS_PADO		AE30	PS_PADO (crystal pad output for MPSoC built-in RTC)

Table 21: Module Clock Resources

2.12 Reset

The power-on reset signal (POR) and the PS system reset signal (SRST) of the MPSoC device are available on the module connector X.

Pulling PS_POR# low resets the MPSoC device, the PS Ethernet and the USB PHYs, the QSPI and eMMC flash devices and the secure EEPROM. Refer to the Enclustra Module Pin Connection Guidelines [10] for general rules regarding the connection of reset pins.

PS_SRST# is connected solely to the MPSoC device and can be used for debugging.

For details on the functions of the PS_POR_B and PS_SRST_B signals refer to the Zynq UltraScale+ MPSoC Technical Reference Manual [15].

In addition to these reset signals, an additional signal (PS_RST#_OUT) is available on an MIO pin and can be used to reset the PS peripherals (Ethernet, USB, QSPI flashes, eMMC flash, secure EEPROM), and an additional signal on the PL side (PL_RST#) that can be used to reset the PL Ethernet PHY.

Table 22 presents the available reset signals. PS_POR# and PS_SRST#, have on-board 4.7 kΩ pull-up resistors to V_IO_CFG.

Signal Name	Connector Pin	Package Pin	FPGA Pin Name	Description
PS_POR#	X-C59	T29	PS_POR_B	Power-on reset
PS_SRST#	X-C58	W29	PS_SRST_B	System reset
PS_RST#_OUT	-	AP22	PS_MIO43	PS peripherals reset
PL_RST#	-	K12	IO_L8N_HDGC_AD4N_90	PL peripherals reset

Table 22: Reset Resources

All the reset signals are automatically asserted if PWR_GOOD is low.

2.13 LEDs

There are four active-low user LEDs on the Andromeda XZU90 module - two of them are connected to the PS and two are connected to the PL.

LED	Signal Name	Signal Location	Remarks
0	PS_MIO33_PERSTPS#_LED0#	AK21 (PS_MIO33)	User function/active-low, shared with PS PCIe PERST signal
1	PS_MIO32_PERSTPL#_LED1#_R	AK20 (PS_MIO32)	User function/active-low, shared with PL PCIe PERST signal
2	LED2#	L12 (IO_L6N_HDGC_AD6N_90)	User function/active-low
3	LED3#	L13 (IO_L6P_HDGC_AD6P_90)	User function/active-low

Table 23: User LEDs

The module is also equipped with two status LEDs, which offer details on the configuration process for debugging purposes. The status signals are available on the module connector.

LED	PS Signal Name	PS Signal Location	Module Conn. Pin	Remarks
E	PS_ERROR	R30 (PS_ERROR_OUT)	X-B58	Refer to Zynq UltraScale+ MPSoC Technical Reference Manual [15]
S	PS_STATUS	T30 (PS_ERROR_STATUS)	X-B59 (assembly option, not connected by default)	Refer to Zynq UltraScale+ MPSoC Technical Reference Manual [15]

Table 24: Status LEDs

2.14 DDR4 SDRAM

There is a single DDR4 SDRAM channel on the Andromeda XZU90 module attached directly to the PS side and is available only as a shared resource to the PL side.

The DDR4 SDRAM is connected to PS I/O bank 504. The memory configuration on the Andromeda XZU90 module supports ECC error detection and correction; the correction code type used is single bit error correction and double bit error detection (SEC-DED).

Five 16-bit memory chips are used to build a 72-bit wide memory (8 bits are unused): 64 bits for data and 8 bits for ECC.

The maximum memory bandwidth on the Andromeda XZU90 module is:
2400 Mbit/sec × 64 bit = 19200 MB/sec

2.14.1 DDR4 SDRAM Type

Table 25 describes the memory availability and configuration on the Andromeda XZU90 module.

Module	Density	Configuration
AM-XZU90-D12E	8 Gbit	512 M × 16 bit
AM-XZU90-D13E	16 Gbit	1 G × 16 bit

Table 25: DDR4 SDRAM Characteristics

2.14.2 Signal Description

Refer to the Andromeda XZU90 Module FPGA Pinout Excel Sheet [4] for detailed information on the DDR4 SDRAM connections.

2.14.3 Termination

> **Tip**
>
> No external termination is implemented for the data signals on the Andromeda XZU90 module. Enclustra strongly recommends enabling the on-die termination (ODT) feature of the DDR4 SDRAM device.

2.14.4 Parameters

Table 26 shows the parameters of the PS DDR4 SDRAM to be set in the Vivado project such that it corresponds to the reference design [2] of the Andromeda XZU90 module.

Parameter	Value
Memory type	DDR4
DRAM bus width	64 bit
ECC	Enabled
DRAM chip bus width	16 bit
DRAM chip capacity	8192 Mbit
Bank group address count	1
Bank address count	2
Row address count	16
Column address count	10
Speed bin	DDR4 2400T
Operating frequency	1200 MHz
CAS latency	17
CAS write latency	12
Additive latency	0
RAS to CAS delay	17
Precharge time	17
tRC	46.16 ns
tRASmin	32 ns
tFAW	30 ns

Table 26: DDR4 SDRAM Parameters

2.15 QSPI Flash

The Andromeda XZU90 module is equipped with two QSPI flash devices in a dual parallel configuration.

The QSPI flash can be used to boot the PS, and to store the FPGA bitstream, ARM application code and other user data.

2.15.1 QSPI Flash Characteristics

Table 27 describes the memory availability and configuration on the Andromeda XZU90 module.

As there are two QSPI flash chips assembled on the Andromeda XZU90 module, type "dual parallel" must be selected when programming the flash from Vivado tools.

Flash Type	Size	Manufacturer
S25FL512S	512 Mbit	Cypress (Spansion)

Table 27: QSPI Flash Type

> **Tip**
>
> Different flash memory devices may be assembled in future revisions of the Andromeda XZU90 module. Any flash memory with a different speed and temperature range fulfilling the requirements of the module variant may be used.

2.15.2 Signal Description

The QSPI flash chips are connected to the PS MIO pins 0-5 and PS MIO pins 7-12 and can be programmed via the MPSoc or JTAG.

The reset of the QSPI flash is connected to the PS_POR# and PS_RST#_OUT reset signal.

Refer to Section 3 for details on programming the flash memory.

2.15.3 Configuration

The QSPI flash supports up to 50 MHz operation for standard read. For fast, dual and quad read speed values, refer to the flash device datasheet.

Note that the "Feedback Clk" option on pin MIO6 must be enabled in the Zynq configuration for clock rates higher than 40 MHz.

Refer to the Zynq UltraScale+ MPSoC Technical Reference Manual [15] for details on booting from the QSPI flash.

2.15.4 QSPI Flash Corruption Risk

There have been cases in which it was observed that the content of the flash device got corrupted. According to Cypress, this issue is caused by power loss during the Write Register (WRR) command. The most common reason to use the WRR command is to turn the QUAD bit ON or OFF - this operation takes place usually at the beginning of the boot process. If required, the bootloader code can be adjusted to set the QUAD bit to a fixed value, without invoking this command during boot.

For additional information on this issue, refer to the Cypress documentation and forum discussions [21], [22].

2.16 eMMC Flash

The eMMC flash can be used to boot the PS, and to store the FPGA bitstream, ARM application code and other user data.

2.16.1 eMMC Flash Characteristics

The Andromeda XZU90 module is equipped with a 16 GB eMMC flash.

> **Tip**
>
> Different flash memory devices may be assembled in future revisions of the Andromeda XZU90 module. Any flash memory with a different speed and temperature range fulfilling the requirements of the module variant may be used.

2.16.2 Signal Description

The eMMC flash signals are connected to the MIO pins 13-22 for 8-bit data transfer mode. The command signal has a 10 kΩ pull-up resistor to 1.8 V and the data lines have 47 kΩ pull-up resistors to 1.8 V.

2.17 SD Card

An SD card can be connected to the PS MIO pins 39-51. The corresponding MIO pins are available on module connector X. Information on SD card boot mode is available in Section 3.8.

External pull-ups are needed for SD card operation. Depending on the selected voltage for V_IO_CFG, a level shifter to 3.3 V may be required (some level shifters also have built-in pull-ups).

SD version 3.0 is supported on Andromeda XZU90 module. In this case, an SD 3.0 compliant level shifter is required on the base board and V_IO_CFG must be set to 1.8 V. For further information on the SD Card interface, refer to [15].

2.18 Gigabit Ethernet (PS)

One of two 10/100/1000 Mbit Ethernet PHYs that are available on the Andromeda XZU90 module is connected to the PS via RGMII interface. The second one is connected to PL via RGMII.

2.18.1 Ethernet PHY Characteristics

Table 28 describes the Ethernet PHY (PS) device type assembled on the Andromeda XZU90 module.

PHY Type	Manufacturer	Type
KSZ9031RNX	Microchip	10/100/1000 Mbit

Table 28: Gigabit Ethernet PHY (PS) Type

2.18.2 Signal Description

Ethernet PHY 0 is connected to ETH 3 controller from the PS I/O bank 502. The interrupt output of the PS Ethernet PHY is connected to the I2C interrupt line, available on pin C49 of connector X.

2.18.3 External Connectivity

The Ethernet signal lines can be connected directly to the magnetics. Refer to the Enclustra Module Pin Connection Guidelines [10] for details regarding the connection of Ethernet signals.

2.18.4 MDIO Address

The MDIO address assigned to PHY 0 is 3, and the PHY can be configured via MIO pins 76-77.

2.18.5 PHY Configuration

The configuration of the Ethernet PHY is bootstrapped when the PHY is released from reset. Make sure all I/Os on the RGMII interface are initialized and all pull-up or pull-down resistors are disabled at that moment.

The bootstrap options of the Ethernet PHYs are set as indicated in Table 29.

Strap Input	Signal Value	Description
MODE[3-0]	1110	RGMII mode: advertise all capabilities (10/100/1000, half/full duplex) except 1000Base-T half duplex.
PHYAD[2-0]	011	MDIO address 3
CLK125_EN	0	125 MHz clock output disabled
LED_MODE	1	Single LED mode

Table 29: Gigabit Ethernet PHY (PS) Configuration - Bootstraps

For the Ethernet PHY configuration via the MDIO interface, the MDC clock frequency must not exceed 2 MHz.

The PHY is configured in single LED mode with active-low LEDs 1 and 2.

2.18.6 RGMII Delays Configuration

The Ethernet PHY (PS) is connected directly to the hard MAC controller present in the MPSoC device. In order to achieve the best sampling eye for the RX and TX data, it is recommended to adjust the pad skew delays as specified in Table 30. These values have been successfully tested on Enclustra side.

The delays can be adjusted by programming the RGMII pad skew registers of the Ethernet PHY. Refer to the PHY datasheet for details.

PHY Register Name	Register Value [binary]	Delay Value
RXD0-RXD3	0111	0 ps
RX_DV	0111	0 ps
RX_CLK	01111	0 ps
TXD0-TXD3	0111	0 ps
TX_EN	0111	0 ps
GTX_CLK	11110	900 ps

Table 30: Gigabit Ethernet PHY (PS) Configuration - RGMII Delays

2.19 Gigabit Ethernet (PL)

2.19.1 Ethernet PHY Characteristics

Table 31 describes the Ethernet PHY (PL) device type assembled on the Andromeda XZU90 module.

PHY Type	Manufacturer	Type
KSZ9031RNX	Microchip (Micrel)	10/100/1000 Mbit

Table 31: Gigabit Ethernet PHY (PL) Type

2.19.2 Signal Description

Ethernet PHY 1 is connected to FPGA HD bank 90, for usage with a soft Ethernet MAC IP core providing RGMII interface for communication with the PHY.

Alternatively, the Ethernet MAC from the PS can be used and mapped to EMIO pins. A GMII to RGMII converter must be used to convert the bus to the appropriate interface standard. The Xilinx GMII to RGMII converter cannot be used on the Andromeda XZU90 module because this IP core includes I/O delay macros that are not supported in HD I/O banks (where the Ethernet pins are mapped). A suitable GMII to RGMII converter is included in the reference design.

The reset pin of the Ethernet PHY is connected to FPGA HD bank 90, pin K12, and is by default inactive. The interrupt output of the Ethernet PHY is connected to FPGA pin P14 from the same bank.

2.19.3 External Connectivity

The Ethernet signal lines can be connected directly to the magnetics. Refer to the Enclustra Module Pin Connection Guidelines [10] for details regarding the connection of Ethernet signals.

2.19.4 MDIO Address

The MDIO address assigned to PHY 1 is 7, and the PHY can be configured via FPGA pins L14 and L15 from HD bank 90.

2.19.5 PHY Configuration

The configuration of the Ethernet PHY is bootstrapped when the PHY is released from reset. Make sure all I/Os on the RGMII interface are initialized and all pull-up or pull-down resistors are disabled at that moment.

The bootstrap options of the Ethernet PHYs are set as indicated in Table 32.

Strap Input	Signal Value	Description
MODE[3-0]	1110	RGMII mode: advertise all capabilities (10/100/1000, half/full duplex) except 1000Base-T half duplex.
PHYAD[2-0]	111	MDIO address 7
CLK125_EN	0	125 MHz clock output disabled
LED_MODE	1	Single LED mode

Table 32: Gigabit Ethernet PHY (PL) Configuration - Bootstraps

For the Ethernet PHY configuration via the MDIO interface, the MDC clock frequency must not exceed 2 MHz.

The PHY is configured in single LED mode with active-low LEDs 1 and 2.

2.19.6 RGMII Delays Configuration

The Ethernet PHY (PL) is connected to the PL side of the MPSoC device, to be used in combination with a soft MAC controller. In order to achieve the best sampling eye for the RX and TX data, it is recommended to adjust the timing constraints of the FPGA pins and/or the pad skew delays of the Ethernet PHY. Refer to the Ethernet PHY datasheet for details on how to program the RGMII pad skew registers.

In the Andromeda XZU90 module reference design the RGMII delays are set through timing constraints, additional the pad delays are configured to provide 2 ns delay on the TX clock signal.

2.20 USB 2.0

A USB 2.0 PHY is available on the Andromeda XZU90 module and connected to the PS to MIO bank 502. The USB PHY can be configured to host, device or On-The-Go (OTG) mode.

2.20.1 USB PHY Characteristics

Table 33 describes the USB PHY device type assembled on the Andromeda XZU90 module.

PHY Type	Manufacturer	Type
USB3320C	Microchip	USB 2.0 PHY

Table 33: USB 2.0 PHY Type

2.20.2 Signal Description

The ULPI interface for the USB 2.0 PHY is connected to MIO pins 52-63 for use with the integrated USB controller.

2.21 USB 3.0

Xilinx Zynq UltraScale+ devices feature two built-in USB 3.0 controllers and PHYs, configurable as host or device. The PHY interface used by the USB 3.0 controller is PIPE3, supporting a 5 Gbit/s data rate in host or device mode. The interface of each USB 3.0 controller uses one of the PS GTR lanes.

A 100 MHz differential clock is available on the module and connected to PS_MGTREFCLK2 pins, to be used as a reference clock for the USB 3.0 interface. It is also possible to provide another reference clock from the base board to the MGTPS_REFCLK* pins.

Details on the built-in USB 2.0/3.0 controller and on the usage of the PS GTR lanes are available in the Zynq UltraScale+ MPSoC Technical Reference Manual [15] and in the Zynq UltraScale+ MPSoC Overview [19].

Figure 11 shows an example of a USB 3.0 implementation using the built-in Xilinx USB 3.0 interface and the USB 2.0 signals from the PHY, all routed to a USB 3.0 connector on the base board.

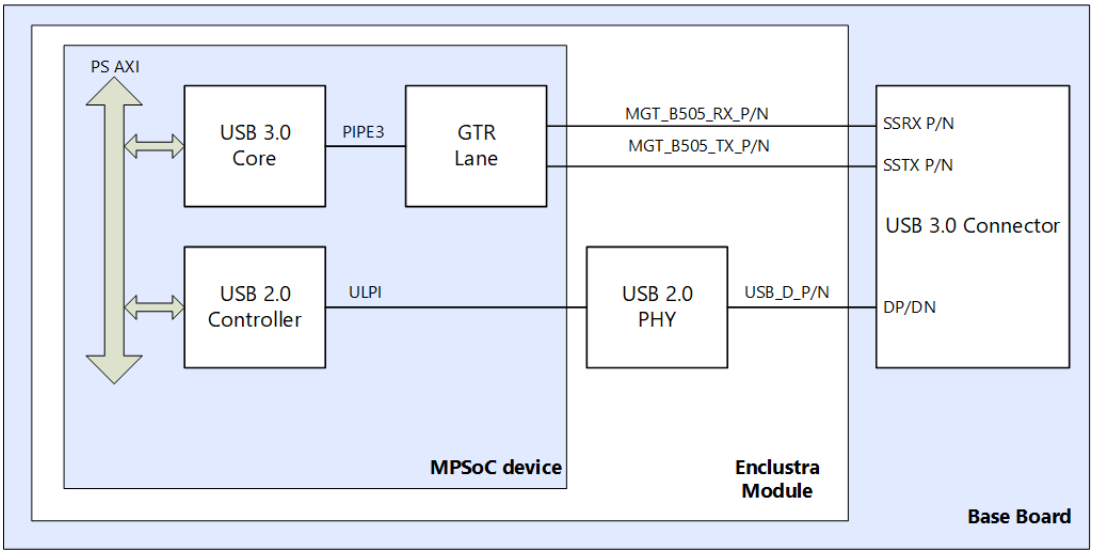

Figure 11: USB 3.0 Implementation Example

2.22 Display Port

Xilinx Zynq UltraScale+ devices feature a built-in DisplayPort controller and PHY, supporting up to two lanes at a 5.4 Gbit/s line rate. Each lane is represented by one of the PS GTR lines, available on the module connector.

A 27 MHz differential clock is available on the module and connected to PS_MGTREFCLK3 pins, to be used as a reference clock for the DisplayPort interface. It is also possible to provide another reference clock from the base board to the MGTPS_REFCLK* pins.

For the DisplayPort AUX port, MIO pins 34-37 are available on the module connector and can be used on the baseboard for DP implementation.

Details on the built-in DisplayPort controller and on the usage of the PS GTR lanes is available in the Zynq UltraScale+ MPSoC Technical Reference Manual [15] and in the Zynq UltraScale+ MPSoC Overview [19].

2.23 Real-Time Clock (RTC)

Zynq UltraScale+ devices include an internal real-time clock. More information on the RTC is available in the Zynq UltraScale+ MPSoC Technical Reference Manual [15].

The RTC crystal pad input and crystal pad output are connected on the Andromeda XZU90 module to a 32.768 kHz oscillator.

In order to use the built-in RTC, a suitable voltage supply needs to be provided to the VCC_PSBATT pin which is connected directly to pin A59 on module connector X.

2.24 Secure EEPROM

The secure EEPROM is used to store the module type and serial number, as well as the Ethernet MAC address and other information. It is connected to the Management (MGMT) I2C bus. Refer to Section 4 for more information on the I2C communication.

The secure EEPROM must not be used to store user data. Refer to Section 4.4 for details on the content of the EEPROM.

2.24.1 EEPROM Characteristics

Table 34 describes the EEPROM devices assembled on the Andromeda XZU90 module.

Type	Manufacturer
ATSHA204A-MAHDA-T (default)	Microchip Technology /Atmel
ATECC608A-MAHDA-S (assembly option)	Microchip Technology /Atmel
SLS32AIA010MLUSON10XTMA2 (default)[6]	Infineon Technologies

Table 34: EEPROM Type

An example demonstrating how to read data from the EEPROM is included in the Andromeda XZU90 module reference design [2].

[6] This device is connected in parallel to the same I2C bus. It is currently not used by Enclustra and is reserved for future use.

3 Device Configuration

3.1 Configuration Signals

The PS of the MPSoC needs to be configured before the FPGA logic can be used. Xilinx Zynq devices need special boot images to boot from QSPI flash, eMMC flash or SD card. For more information, refer to the Zynq UltraScale+ MPSoC Technical Reference Manual [15].

Table 35 describes the most important configuration pins and their location on the module connector. These signals allow the MPSoC to boot from QSPI flash, eMMC flash or SD card.

Signal Name	MPSoC Pin Type	Mod. Conn. Pin	Description	Comments
PS_DONE	PS_DONE	X-C53	MPSoC device configuration done	4.7 kΩ pull-up to VCC_CFG_MIO
PS_POR#	PS_POR_B	X-C59	MPSoC power-on reset	4.7 kΩ pull-up to V_IO_CFG
PS_SRST#	PS_SRST_B	X-C58	MPSoC system reset	4.7 kΩ pull-up to V_IO_CFG
BOOT_MODE0	PS_MODE0	X-C54	Boot mode selection	4.7 kΩ pull-down
BOOT_MODE1	PS_MODE1	X-C55	Boot mode selection	4.7 kΩ pull-up to V_IO_CFG
BOOT_MODE2	PS_MODE2	X-C56	Boot mode selection	4.7 kΩ pull-down
BOOT_MODE3	PS_MODE3	X-C57	Boot mode selection	4.7 kΩ pull-down

Table 35: MPSoC Configuration Pins

NOTICE

Damage to the device

- Only allow the signals PS_POR# and PS_SRST# to be driven low.
- Do not drive PS_POR# or PS_SRST# to a logic high level.
- Do not drive onto the PS_DONE pin on the base board.

3.2 Pull-Up During Configuration

The Pull-Up During Configuration signal (PUDC) is pulled to GND on the module; as PUDC is an active-low signal, all FPGA I/Os will have the internal pull-up resistors enabled during device configuration.

If the application requires the pull-up during configuration to be disabled, this can be achieved by removing R1017 component and by mounting R1013 - in this configuration the PUDC pin is connected to 1.8 V.

Figure 12 illustrates the configuration of the I/O signals during power-up. Figure 13 indicates the location of the pull-up/pull-down resistors on the module PCB - lower right part on the bottom view drawing.

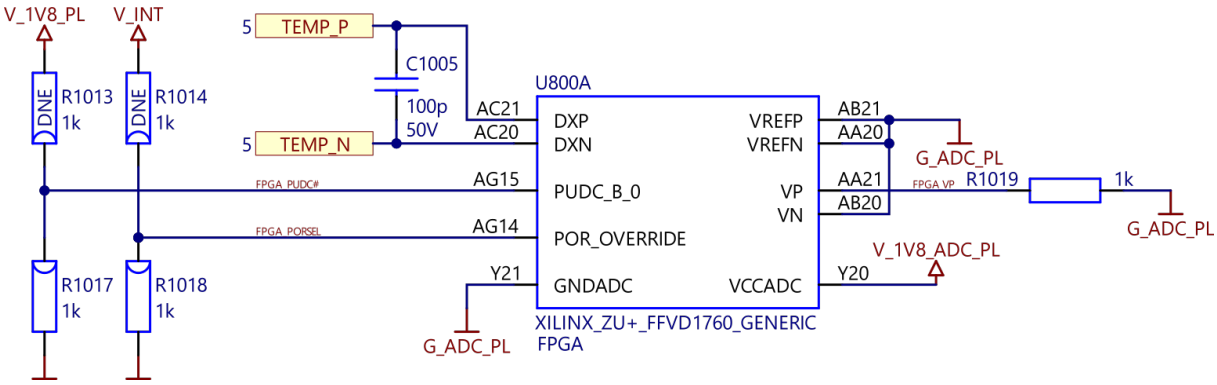

Figure 12: Pull-Up During Configuration (PUDC) and Power-on Reset Delay Override (PORSEL)

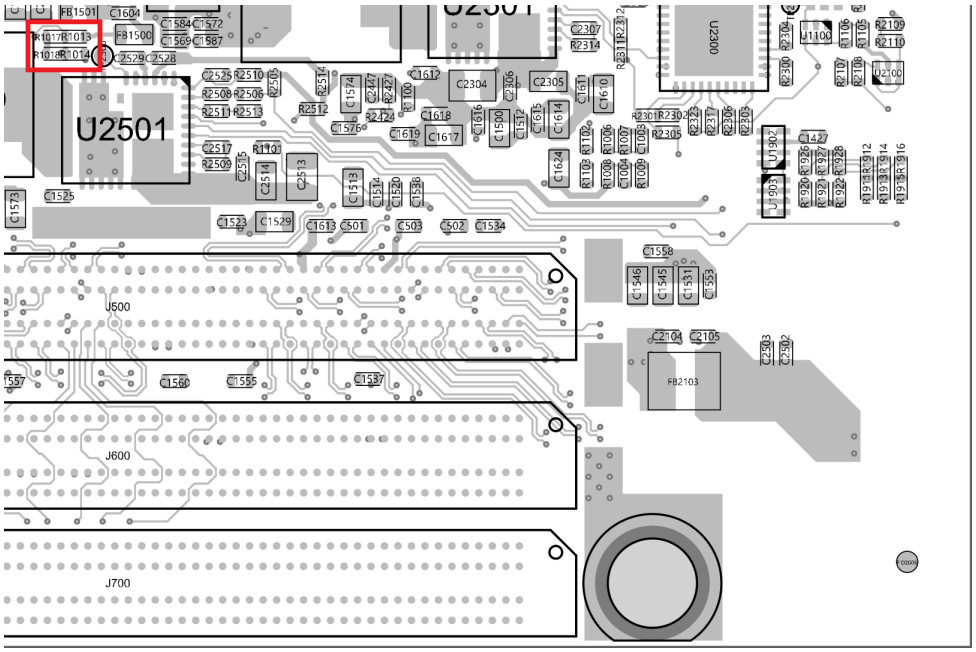

Figure 13: Pull-Up During Configuration (PUDC) and Power-on Reset Delay Override (PORSEL) Resistors

For details on the PUDC signal, refer to the Zynq UltraScale+ MPSoC Technical Reference Manual [15].

3.3 Power-on Reset Delay Override

The power-on reset delay override MPSoC signal (POR_OVERRIDE) is pulled to GND on the module, setting the PL power-on delay time to the default standard time.

If the application requires faster PL power-on delay time, this can be achieved by removing R1018 component and by mounting R1014.

Figure 12 illustrates the configuration of the POR_OVERRIDE signal. Figure 13 indicates the location of the pull-up/pull-down resistors on the module PCB - lower right part on the bottom view drawing.

For details on the POR_OVERRIDE signal, refer to the Zynq UltraScale+ MPSoC Technical Reference Manual [15].

3.4 Boot Mode

The boot mode can be selected via four signals available on the module connector.

Table 36 describes the available boot modes on the Andromeda XZU90 module.

BOOT MODE3	BOOT MODE2	BOOT MODE1	BOOT MODE0	Description
0	0	0	0	JTAG boot mode
0	0	1	0	Boot from QSPI flash (default)
0	1	0	1	Boot from SD card
0	1	1	0	Boot from eMMC flash
1	1	1	0	Boot from SD card (with an external SD 3.0 compliant level shifter; only available when V_IO_CFG is 1.8 V)
0	1	1	1	USB 2.0 DFU boot mode

Table 36: Boot Modes

3.5 JTAG

The Zynq UltraScale+ devices include two separate JTAG controllers: the Zynq UltraScale+ TAP and the ARM DAP. The first one uses the PS dedicated JTAG pins and has access to both PS and PL and the second one uses the PS PJTAG pins and is used for loading programs, system test, and PS debug.

Details on JTAG and on system test and debug are available in the Zynq UltraScale+ MPSoC Technical Reference Manual [15].

Certain Xilinx tool versions support QSPI flash programming via JTAG only when JTAG boot mode is used. Alternatively, the QSPI flash can be programmed in u-boot or Linux by the SPI controller in the PS.

3.5.1 JTAG on Module Connector

The PL and the PS JTAG interfaces are connected into one single chain available on the module connector. The PS_JTAG pins are used by the Zynq UltraScale+ TAP controller - the controller has full functionality only after the PS boot is complete. In order to enable the ARM DAP controller, special commands must be sent to the Zynq UltraScale+ TAP.

The MPSoC device and the flash devices can be configured via JTAG from Xilinx Vitis or Xilinx Vivado Hardware Manager - for this operation, the ARM DAP must be enabled.

Signal Name	Module Connector Pin	PS Dedicated Pin	Resistor
JTAG_TCK	X-D52	PS_JTAG_TCK	4.7 kΩ pull-up to V_IO_CFG
JTAG_TMS	X-D55	PS_JTAG_TMS	4.7 kΩ pull-up to V_IO_CFG
JTAG_TDI	X-D51	PS_JTAG_TDI	4.7 kΩ pull-up to V_IO_CFG
JTAG_TDO	X-D54	PS_JTAG_TDO	4.7 kΩ pull-up to V_IO_CFG

Table 37: JTAG Interface - PL and PS Access and Debug

3.5.2 External Connectivity

JTAG signals can be connected directly on the base board to a JTAG connector. No pull-up/pull-down resistors are necessary. The VREF pin of the programmer must be connected to V_IO_CFG.

It is recommended to add 22 Ω series termination resistors between the module and the JTAG header, close to the source. Refer to the Enclustra Module Pin Connection Guidelines for details on JTAG interface.

3.6 eMMC Boot Mode

In the eMMC boot mode, the PS boots from the eMMC flash located on the module. The flash device is connected to the PS MIO pins 13-22 for 8-bit data transfer mode.

3.7 QSPI Boot Mode

In the QSPI boot mode, the PS boots from the two QSPI flash devices located on the module. The flash devices are connected to the PS MIO pins 0-5 (QSPI0) and PS MIO pins 7-12 (QSPI1).

3.8 SD Card Boot Mode

In the SD card boot mode, the PS boots from the SD card located on the base board. There are two SD card boot modes available on the Andromeda XZU90 module.

The SD boot mode with level shifter is used with Ultra High Speed (UHS) SD cards. The controller will start the communication at 3.3 V and afterwards it will command the card to drop from 3.3 V operation to 1.8 V operation. For this mode, an external SD 3.0 compliant level shifter is required.

For details on SD card boot, refer to the Zynq UltraScale+ MPSoC Technical Reference Manual [15].

3.9 USB 2.0 DFU Boot Mode

The USB boot mode configures the USB controller into device mode and uses the Device Firmware Upgrade (DFU) protocol to communicate with an attached host. For details on USB boot, refer to the Zynq UltraScale+ MPSoC Technical Reference Manual [15].

3.10 eMMC Flash Programming

The eMMC flash can be programmed in u-boot or Linux and formatted in Linux, like a regular SD card. The boot image or independent partition files can be transmitted via Ethernet or copied from another storage device.

Certain Xilinx tool versions support eMMC flash programming via JTAG.

3.11 QSPI Flash Programming via JTAG

The Xilinx Vivado and Vitis software offer QSPI flash programming support via JTAG.

Certain Xilinx tools versions support QSPI flash programming via JTAG only when JTAG boot mode is used. For more information, refer to the Xilinx documentation [15] and support. Alternatively, the QSPI flash can be programmed in u-boot or Linux by the SPI controller in the PS.

4 I2C Communication

4.1 Overview

There are two I2C buses on the Andromeda XZU90 module. They are referred to as "I2C_USER" and "I2C_MGMT". They are connected to the MPSoC device, the EEPROM, the power converters and to the module connector. This allows external devices to read the module type from the EEPROM and allows connecting more devices to the I2C bus.

The I2C clock frequency should not exceed 400 kHz.

> **Tip**
>
> Maximum I2C speed may be limited by the routing path and additional loads on the base board.

> **Tip**
>
> If the I2C traces on the base board are very long, 100 Ω series resistors should be added between module and I2C device on the base board.

4.2 Signal Description

A detailed view on the I2C bus interface is given in Figure 14. Additionally, Table 38 describes the signals of the I2C interfaces.

All signals are pulled up to a voltage of 3.3 V. All signals must be connected to open collector outputs and must not be driven high from any source. I2C_INT# is an input to the MPSoC and must not be driven from the MPSoC device.

Level shifters are used between the I2C buses and the MPSoC pins, as I/O banks 500 and 90 are supplied with 1.8 V and bank 501 is supplied with V_IO_CFG. Ensure that all pins are configured correctly and no pull-down resistors are enabled.

The control of the PL Buck Converter is configurable between the I2C_USER and the I2C_MGMT data bus through a different resistor assembly option.

In the default assembly variant, the PL Buck converter is connected to the I2C_MGMT data bus.

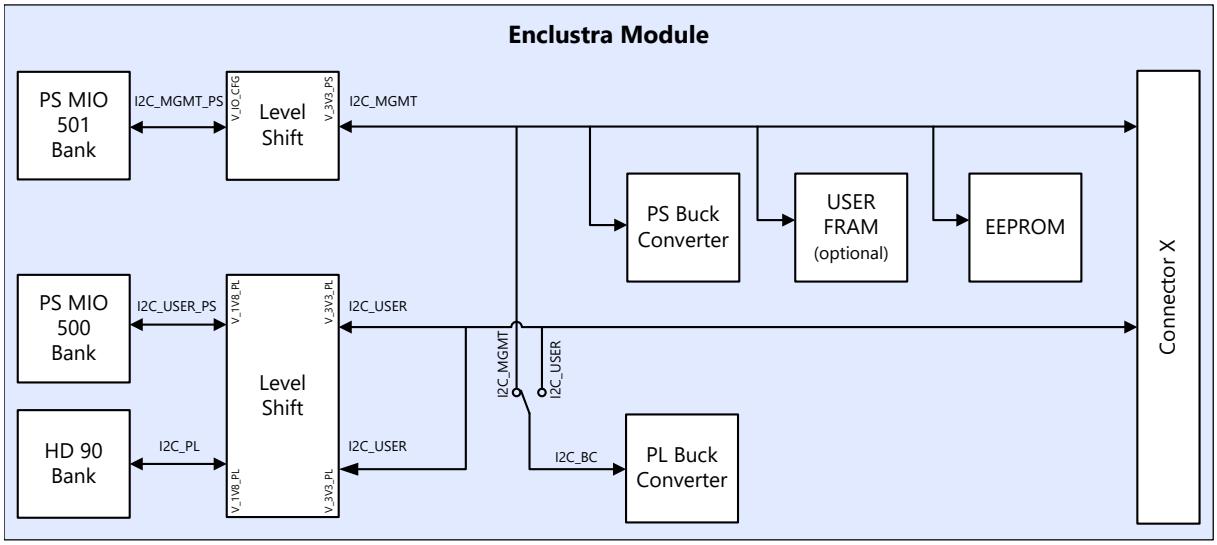

Figure 14: I2C Interface Overview

Signal Name	PS Pin	PL Pin	Connector Pin
I2C_USER_SDA	AN28 (MIO25)	R15	X-D34
I2C_USER_SCL	AN26 (MIO24)	T15	X-D33
I2C_USER_INT#	AN25 (MIO23)	P14	X-D35
I2C_MGMT_SDA	AJ22 (MIO31)	-	X-C51
I2C_MGMT_SCL	AJ21 (MIO30)	-	X-C50
I2C_MGMT_INT#	AM21 (MIO38)	-	X-C49

Table 38: I2C Signal Description

4.3 I2C Address Map

Table 39 describes the addresses for several devices connected on I2C MGMT bus.

Address (7-bit)	Description	Manufacturer Part Number
0x64	Secure EEPROM (default option, refer to Section 2.24)	ATSHA204A-MAHDA-T
0x64	Secure EEPROM (assembly option, refer to Section 2.24)	ATECC608A-MAHDA-S
0x30	Secure EEPROM (reserved for future use, refer to Section 2.24)	SLS32AIA010MLUSON10XTMA2
0x57	Optional USER FRAM	MB85RC64TA
0x13	PS Buck Converter 0	IRPS5401MTRPBF
0x10	PL Buck Converter 1	IR35215MTRPBF
0x1D	PL Buck Converter 2	IRPS5401MTRPBF
0x1F	PL Buck Converter 3	IRPS5401MTRPBF

Table 39: I2C Addresses

4.4 Secure EEPROM

The secure EEPROM is used to store the module serial number and configuration. An example demonstrating how to read the module information from the EEPROM memory is included in the Andromeda XZU90 module reference design.

> **Tip**
>
> Any attempt to write data to the secure EEPROM causes the warranty to be rendered void.

4.4.1 Memory Map

Address	Length (bits)	Description
0x00	32	Module serial number
0x04	32	Module product information
0x08	32	Module configuration
0x0C	8	Module configuration
0x0D	24	Module configuration
0x10	48	Ethernet MAC 0 address
0x16	48	Reserved
0x1C	32	Reserved

Table 40: EEPROM Sector 0 Memory Map

Module Serial Number

The module serial number is a unique 32-bit number that identifies the module. It is stored using big-endian byte order (MSB on the lowest address).

Module Product Information

This field indicates the type of module and hardware revision.

Module	Product Family	Reserved	Revision	Product Information
Andromeda XZU90 module	0x0338	0x[XX]	0x[YY]	0x0338 [XX][YY]

Table 41: Product Information

Module Configuration

Addr.	Bits	Comment	Min. Value	Max. Value	Comment
0x08	7-4	MPSoC type	0	1	See MPSoC type table (Table 43)
	3-0	MPSoC device speed grade	1	3	
0x09	7-6	Temperature range	0	2	See temperature range table (Table 44)
	5	Power grade	0 (Normal)	1 (Low power)	
	4-3	Gigabit Ethernet port count	0	2	
	2-1	QSPI flash interface	0	2	See QSPI flash type (Table 45)
	0	DDR4 PS ECC enabled	0 (No)	1 (Yes)	
0x0A	7-2	Reserved	-	-	
	1-0	USB 2.0 port count	0	1	
0x0B	7-4	DDR4 RAM (PS) size (GB)	0 (0 GB)	3 (4 GB)	Resolution = 1 GB
	3-0	Reserved	-	-	
0x0C	7-4	eMMC flash size (GB)	0 (0 GB)	5 (16 GB)	Resolution = 1 GB
	3-0	QSPI flash size (MB)	0 (0 MB)	8 (128 MB)	Resolution = 1 MB
0x0D	7-4	User FRAM size (kB)	0 (0 kB)	4 (8 kB)	Resolution = 1 kB
	3-0	Reserved	-	-	

Table 42: Module Configuration

The memory sizes are defined as Resolution$\times 2^{(Value-1)}$, for example:

- DRAM = 0: none
- DRAM = 1: 1 GB
- DRAM = 2: 2 GB
- DRAM = 3: 4 GB

Table 43 shows the available MPSoC types.

Value	MPSoC Device Type
0	XCZU17EG
1	XCZU19EG

Table 43: MPSoC Device Types

Table 44 shows the available temperature ranges.

Value	Module Temperature Range
0	Commercial
1	Extended
2	Industrial

Table 44: Module Temperature Range

Table 45 shows the QSPI interface configuration options.

Value	Interface Type
0	Single
1	Dual parallel
2	Dual stacked

Table 45: QSPI flash interface

Ethernet MAC Address

The Ethernet MAC address is stored using big-endian byte order (MSB on the lowest address). Each module is assigned two sequential MAC addresses; only the lower one is stored in the EEPROM.

5 Operating Conditions

5.1 Absolute Maximum Ratings

Table 46 indicates the absolute maximum ratings for Andromeda XZU90 module. The values given are for reference only. For details, refer to the Zynq UltraScale+ MPSoC, DC and AC Switching Characteristics Datasheet [17].

Parameter	Description	Rating	Unit
V_MOD_PS	Supply voltage (PS) relative to GND	-0.5 to 16	V
V_MOD_PL_[x]	Supply voltage (PL) relative to GND	-0.5 to 16	V
V_BAT	Supply voltage for MPSoC battery-backed RAM and battery-backed RTC	-0.5 to 2	V
V_IO_B91	Output drivers supply voltage relative to GND	-0.5 to 3.4	V
VCC_IO_CFG	Output drivers supply voltage relative to GND	-0.5 to 3.63	V
V_IO_B65 V_IO_B66 V_IO_B69 V_IO_B70 V_IO_B71	Output drivers supply voltage relative to GND	-0.5 to 2.0	V
V_IO	I/O input voltage relative to GND	-0.5 to V_{CCO}+0.5	V
Temperature[7]	Temperature range for extended temperature modules (E)	0 to +85	°C
	Temperature range for industrial modules (I)	-40 to +85	°C

Table 46: Absolute Maximum Ratings

NOTICE

Damage to the device due to overheating

Depending on the user application, the Andromeda XZU90 module may consume more power than can be dissipated without additional cooling measures.

- Ensure that the MPSoC is always adequately cooled by installing a heat sink and/or providing air flow.

[7] The components used on the hardware are specified for the relevant temperature range. The user must provide adequate cooling in order to keep the temperature of the components within the specified range.

5.2 Recommended Operating Conditions

Table 47 indicates the recommended operating conditions for Andromeda XZU90 module. The values given are for reference only. For details, refer to the Zynq UltraScale+ MPSoC, DC and AC Switching Characteristics Datasheet [17].

Parameter	Description	Rating	Unit
V_MOD_PS	Supply voltage (PS) relative to GND	12 V	V
V_MOD_PL_[x]	Supply voltage (PL) relative to GND	12 V	V
V_BAT	Supply voltage for MPSoC battery-backed RAM and battery-backed RTC	1.2 to 1.5	V
V_IO_[x]	Output drivers supply voltage relative to GND	Refer to Section 2.8.5	V
V_IO	I/O input voltage relative to GND	-0.2 to V_{CCO}+0.2	V
Temperature[8]	Temperature range for extended temperature modules (E)	0 to +85	°C
	Temperature range for industrial modules (I)	-40 to +85	°C

Table 47: Recommended Operating Conditions

NOTICE

Damage to the device due to overheating

Depending on the user application, the Andromeda XZU90 module may consume more power than can be dissipated without additional cooling measures.

- Ensure that the MPSoC is always adequately cooled by installing a heat sink and/or providing air flow.

[8] The components used on the hardware are specified for the relevant temperature range. The user must provide adequate cooling in order to keep the temperature of the components within the specified range.

6 Ordering and Support

6.1 Ordering

Use the Enclustra online request/order form for ordering or requesting information:
`http://www.enclustra.com/en/order/`

6.2 Support

Follow the instructions on the Enclustra online support site:
`http://www.enclustra.com/en/support/`

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References

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