Mars ST3 Base Board

User Manual

Purpose

The purpose of this document is to present the characteristics of Mars ST3 base board to the user, and to provide the user with a comprehensive guide to understanding and using the Mars ST3 base board.

Summary

This document first gives an overview of the Mars ST3 base board followed by a detailed description of its features and configuration options. In addition, references to other useful documents are included.

Product Information	Code	Name
Product	MA-ST3	Mars ST3 Base Board

Document Information	Reference	Version	Date
Reference / Version / Date	D-0000-455-001	02	22.07.2021

Approval Information	Name	Position	Date
Written by	HMEY	Design Engineer	06.05.2021
Verified by	RGAE	Design Expert	07.06.2021
Approved by	DIUN	Manager, BU SP	22.07.2021

Copyright Reminder

Document History

Version	Date	Author	Comment
02	22.07.2021	DIUN	Fixed VSEL_IO configuration (Table 22)
01	17.06.2021	HMEY	Version 01

Table of Contents

1 Overview

1.1 General

1.1.1 Introduction

The Mars ST3 base board is equipped with a multitude of I/O connectors to use with Mars family FPGA and SoC modules. The board is well-suited for rapid prototyping and for building FPGA systems, without the need for developing custom hardware.

The board can also be used for production flash programming on Mars modules, or for educational purposes.

This board is specially designed for image processing applications.

The main features of the Mars ST3 base board are:

- Support for USB 3.0 host
- FTDI USB 2.0 High-Speed device controller
- High-speed FPGA and flash programming over USB
- Versatile set of I/O connectivity options
- Ethernet RJ45 connector
- MIPI D-PHY interface (CSI)
- HDMI 1.4b connector
- Mini DisplayPort connector
- microSD card slot
- Optional Watchdog timer
- Simple integration by using a single 12 V voltage supply
- Small solution size

1.1.2 Warranty

Please refer to the General Business Conditions, available on the Enclustra website [1].

1.1.3 RoHS

The Mars ST3 base board is designed and produced according to the Restriction of Hazardous Substances (RoHS) Directive (2011/65/EC).

1.1.4 Disposal and WEEE

The Mars ST3 base board must be properly disposed of at the end of its life. If a battery is installed on the board, it must also be properly disposed of.

The Waste Electrical and Electronic Equipment (WEEE) Directive (2002/96/EC) is not applicable for the Mars ST3 base board.

1.1.5 Safety Recommendations and Warnings

Mars boards are not designed to be “ready for operation” for the end-user. Proper configuration of the hardware before usage is required.

Ensure that the power supply is disconnected from the board before inserting or removing a Mars module, connecting interfaces, or connecting jumpers.

Touching the capacitors of the DC-DC converters can lead to voltage peaks and permanent damage; over-voltage on power or signal lines can also cause permanent damage to the board and to the equipped module.

1.1.6 Electrostatic Discharge

Electronic boards are sensitive to electrostatic discharge (ESD). Please ensure that the product is handled with care and only in an ESD-protected environment.

1.1.7 Electromagnetic Compatibility

The Mars ST3 base board is a Class A product (as defined in IEC 61000-3-2 standard) and is not intended for use in domestic environments. The product may cause electromagnetic interference, for which appropriate measures must be taken.

1.2 Deliverables

- Mars ST3 base board including plastic standoffs
- Mars ST3 base board documentation, available via download:
    - Mars ST3 Base Board User Manual (this document)
    - Mars ST3 Base Board IO Net Length Excel Sheet [3]
    - Mars ST3 Base Board User Schematics (PDF) [4]
    - Mars ST3 Base Board Known Issues and Changes [5]
    - Mars ST3 Base Board 3D Model (PDF) [6]
    - Mars ST3 Base Board STEP 3D Model [7]
    - Mercury Mars Module Pin Connection Guidelines [8]
    - Mars Master Pinout [9]

1.3 Accessories

- Mars FPGA or SoC module
- 12 V DC/2.5 A power supply
- USB 2.0 A to micro-B USB cable

1.4 Design Files

The Altium design files for the Mars ST3 base board are available upon request after signing a design license agreement. Please contact Enclustra for further information.

2 Getting Started

This section contains essential information on using the Mars ST3 base board.

Electrostatic discharge (ESD) may damage the Mars ST3 base board partially or completely. Please follow the relevant guidelines for ESD-safe handling when operating or assembling electronic components.

Before first use of the Mars ST3 base board with a Mars module, the following steps must be followed:

- Mount the module on the module slot on the base board, with the power switched off.
- Set the DIP switches correctly (refer to Section 6.3).
- Set the I/O voltage selection jumpers correctly (refer to Section 5.7).
- Power up the board (refer to Section 5 for power options).

The power supply of the base board must be turned off in the following situations:

- Before changing the position of the I/O voltage selection jumpers
- Before removing the Mars module
- Before connecting or disconnecting peripherals to ANIOS and I/O connectors

Before connecting peripherals, make sure that the corresponding VCC_IO voltage is properly set.

The operating conditions for the Mars ST3 base board and equipped module must conform to the values given in Section 7, and in the relevant section from the Mars module user manual.

3 Board Description

3.1 Block Diagram

The Mars ST3 base board can be used in combination with any Mars module. Depending on the equipped module some features may not be available.

The block diagram of the Mars ST3 base board is shown in Figure 1.

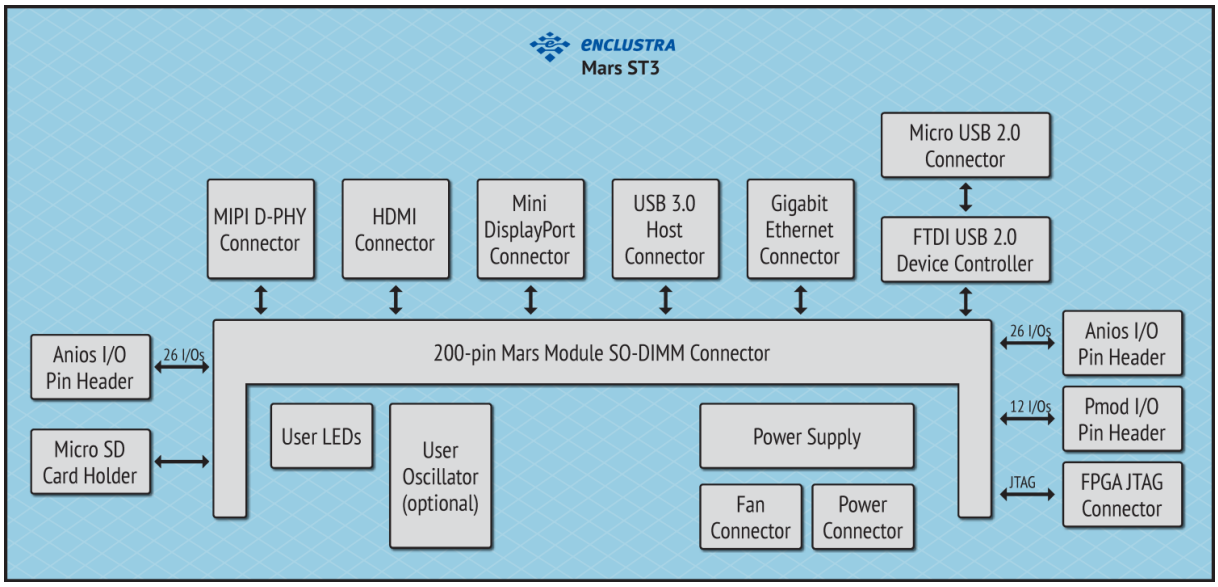


Figure 1: Hardware Block Diagram

3.2 Features

Table 1 describes the features available on the Mars ST3 base board.

Feature	Description
Form factor	100 × 80 mm
System features	Built-in Xilinx JTAG (via USB connection) User oscillator (optional) Watchdog timer (optional)
Memory	microSD card holder
Connectors	USB 3.0 host connector RJ45 Gigabit Ethernet connector Micro USB (FTDI USB 2.0 High-Speed device controller) Mini DisplayPort connector MIPI D-PHY connector (CSI) HDMI 1.4b connector
User I/Os	2 × 40-pin Anios pin header 2 × 12-pin IO connector 1 × user push button (shared with watchdog enable signal)
Supply voltage	12 V DC (internal, external)

Table 1: Base Board Features

Warning!
Please note that the available features depend on the equipped Mars FPGA/SoC module.

3.3 Board Configuration and Product Models

Table 2 describes the standard base board configurations. Custom configurations are available; please contact Enclustra for further information.

Product Model	Features	Temperature Range
MA-ST3-W	Refer to Table 1	-20..+85° C

Table 2: Standard Base Board Configuration

3.4 EN-Numbers and Part Names

Every board is uniquely labeled, showing the EN-number and serial number. An example is presented in Figure 2.

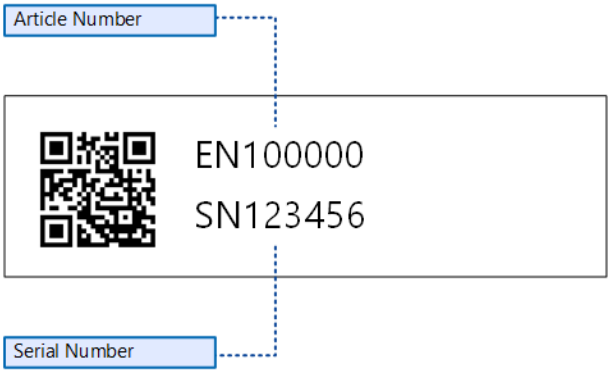


Figure 2: Product Label

The correspondence between EN-number and part name is shown in Table 3. The part name represents the product model, followed by the revision; the R suffix and number represent the revision number.

The revision changes and product known issues are described in the Mars ST3 Base Board Known Issues and Changes document [5].

EN-Number	Part Name
EN102462	MA-ST3-R1.1
EN102556	MA-ST3-X1-R1.1
EN103242	MA-ST3-W-R2

Table 3: EN-Numbers and Part Names

3.5 Top and Bottom Views

3.5.1 Top View

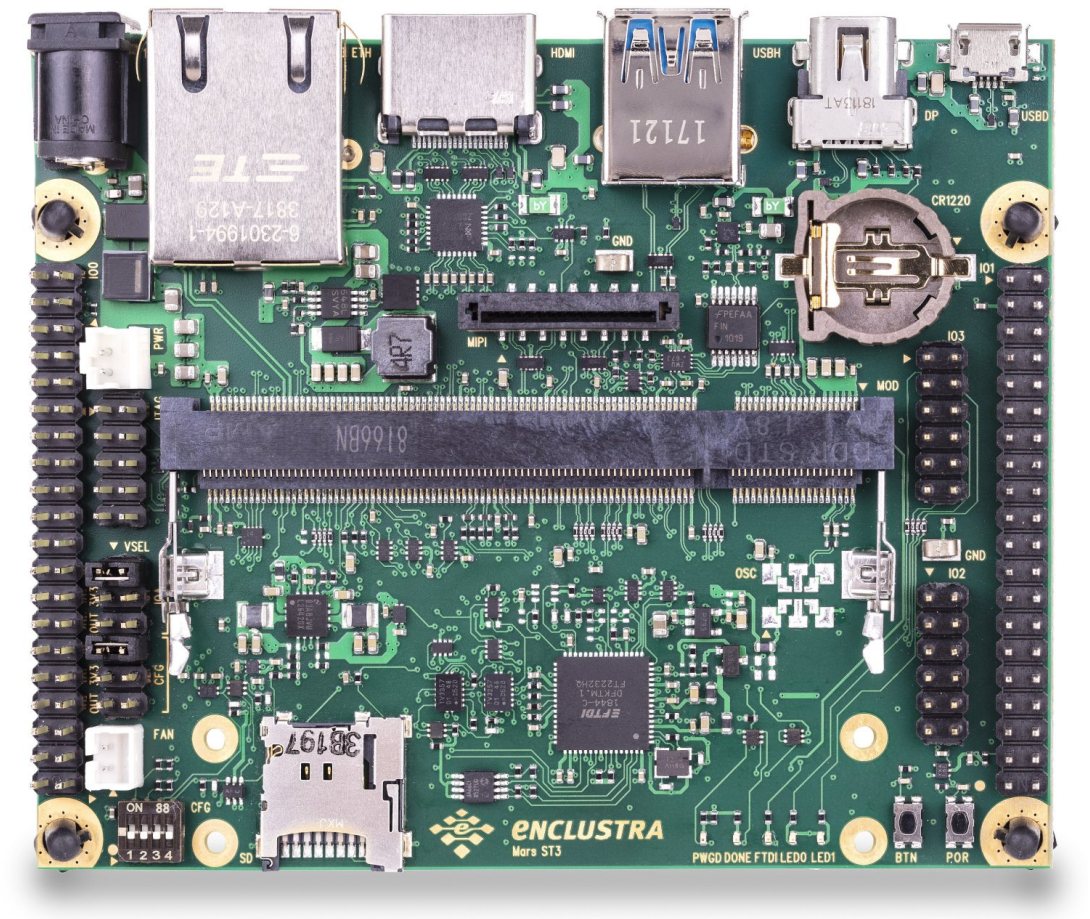


Figure 3: Board Top View

3.5.2 Bottom View

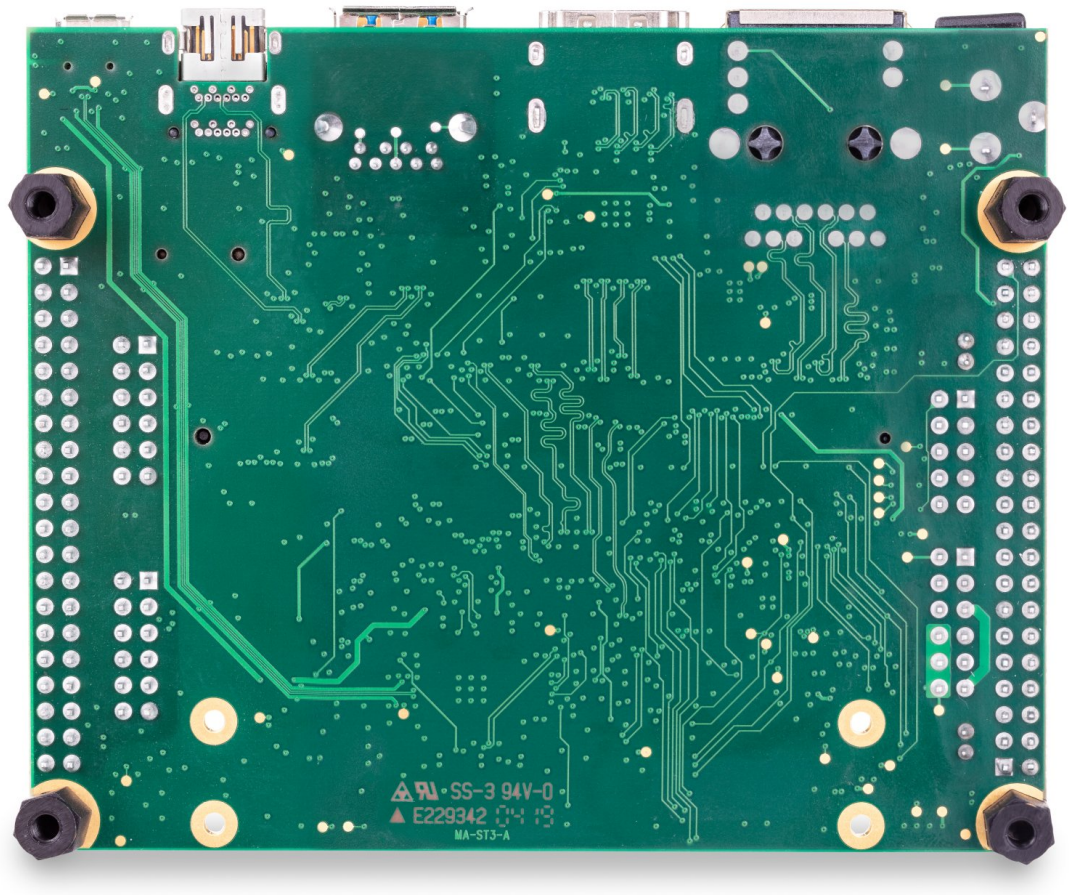


Figure 4: Board Bottom View

Please note that depending on the hardware revision and configuration, the base board may look slightly different than shown in this document.

3.6 Top and Bottom Assembly Drawings

3.6.1 Top Assembly Drawing

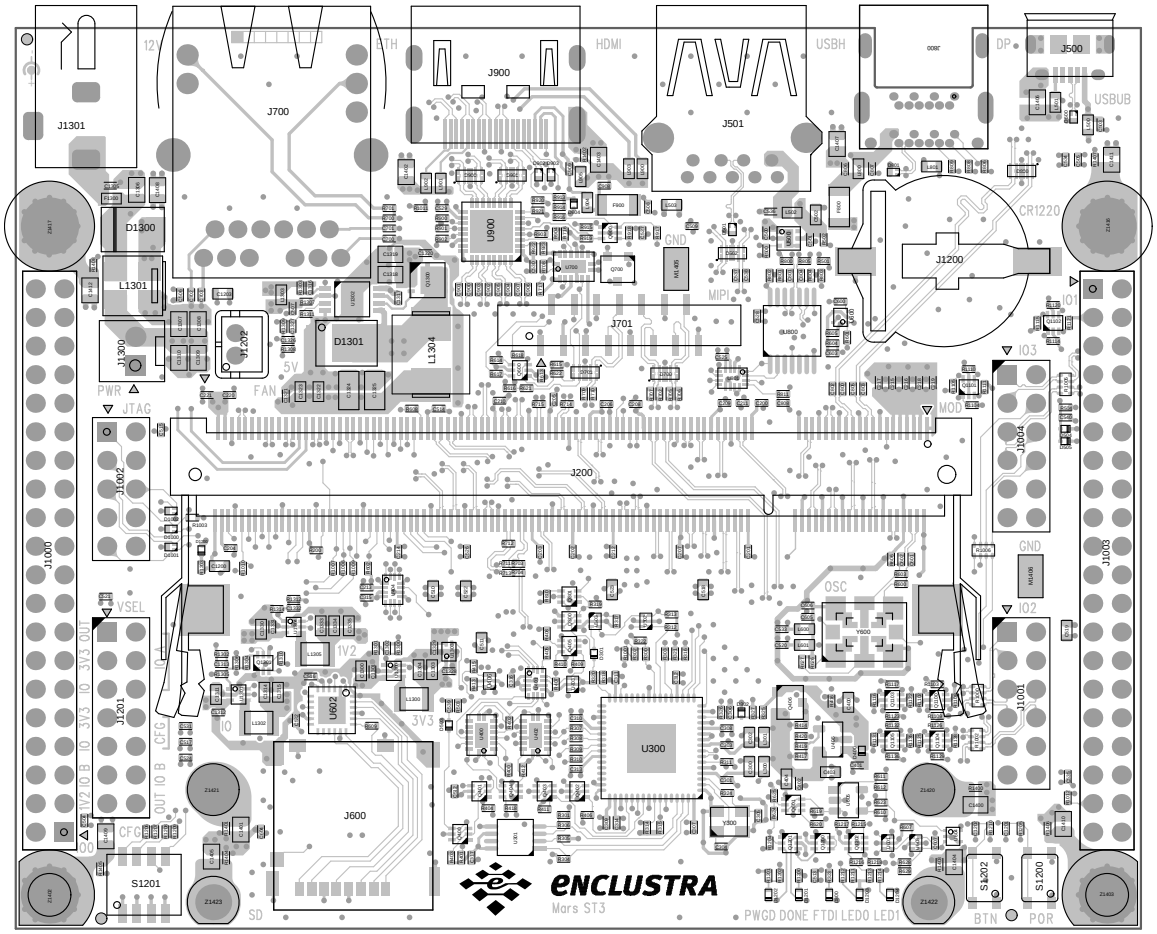


Figure 5: Board Top Assembly Drawing

3.6.2 Bottom Assembly Drawing

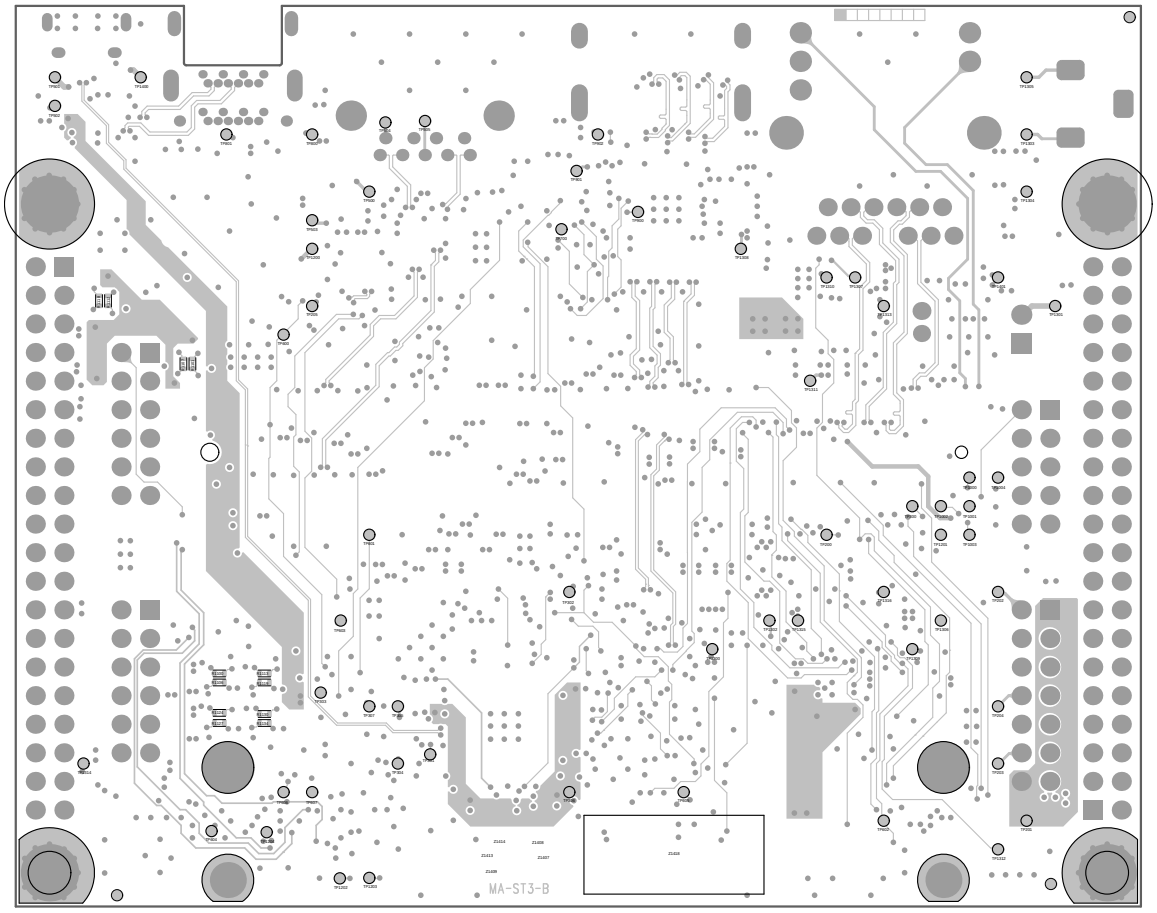


Figure 6: Board Bottom Assembly Drawing

Please note that depending on the hardware revision and configuration, the base board may look slightly different than shown in this document.

3.7 Board Dimensions

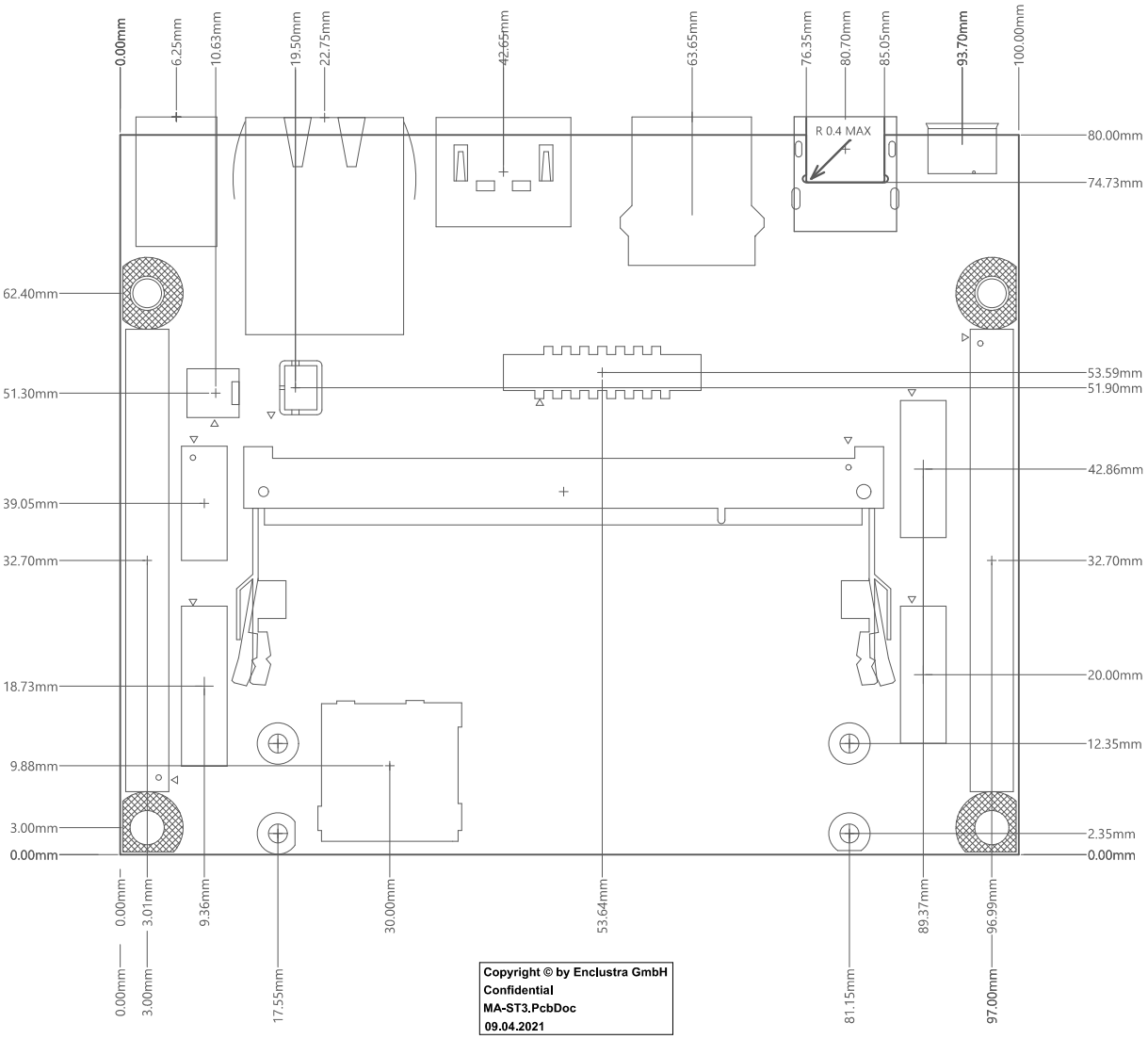


Figure 7: Board Dimensions

3.8 Mechanical Data

Table 4 describes the mechanical characteristics of the Mars ST3 base board. A 3D model (PDF) and a STEP 3D model are available [6], [7].

Symbol	Value
Size	100 × 80 mm
Component height top	11.3 mm
Component height bottom	8 mm plastic standoffs equipped on the bottom side
Weight	64 g (without battery and module)

Table 4: Mechanical Data

3.9 Mechanical Components

Table 5 describes the mechanical components present on the Mars ST3 base board. The listed elements are for reference only. Any other components that meet the requirements may be used.

Product Number	Manufacturer	Description
973080365	Würth Elektronik	4 × plastic spacer bolt with female thread/clip, length 8 mm

Table 5: List of Mechanical Components

4 Connectors Description

4.1 12 V External Power

This connector is used to supply the main VCC input voltage.

Apply only 12 V DC to this connector.

Pin Number	Signal Name	Description
1 (inner)	VCC_MAIN_IN	12 V DC (nominal) input voltage
2 (outer)	GND	Ground

Table 6: External Power Connector

Type	Manufacturer
PJ-102AH	CUI

Table 7: External Power Connector Type

4.2 12 V Internal Power

The Mars ST3 base board can alternatively be powered through the internal power input connector. The 12 V DC power source connected to must be filtered by external power circuitry.

Apply only 12 V DC to this connector.

To avoid any confusion between the DC internal connector and the fan connector, the 12 V internal connector part was been changed starting with revision 2. This section describes only the new part.

Pin Number	Signal Name	Description
1	VCC_MAIN	12 V DC (nominal) input voltage
2	GND	Ground

Table 8: Internal Power Connector

Type	Manufacturer
61900211121	Würth Elektronik

Table 9: Internal Power Connector Type

Table 10 shows an example of a mating part for the internal power connector. This connector is without female crimp contacts, or wires.

Type	Manufacturer
61900311621	Würth Elektronik

Table 10: Mating Part for the Internal Power Connector Pinout

4.3 Fan Connector

This connector can be used to power a 5 V fan. The 2 mm pitch power connector provides access to the power net VCC_5V.

Pin Number	Signal Name	Description
1	VCC_5V	5 V DC voltage source
2	GND	Ground

Table 11: Fan Connector Pinout

Type	Manufacturer
440054-2	TE Connectivity

Table 12: Fan Connector Type

Warning!
Do not short circuit the 5 V power supply, nor use the fan connector as a power input.

Table 13 shows an example of a mating part for the fan/internal power connector. This item is without female crimp contacts, or wires.

Type	Manufacturer
440129-2	TE Connectivity

Table 13: Mating Part for the Fan Connector

4.4 I/O Voltage Selection (J1201)

The I/O voltage selection jumpers are used to configure the VCC_IO_A, VCC_IO_B and VCC_CFG voltages that power the I/O banks of the SoC/FPGA device on the Mars module. Refer to Section 5.7 for details.

Starting with Mars ST3 base board revision 2, the I/O voltage selection connector has 14 pins instead of 12, offering more options for setting the VCC_IO_B voltage.

4.5 Mars Module Connector (J200)

A detailed pinout of the Mars module connector can be found in the Mars Master Pinout [9] and in the Mars ST3 Base Board User Schematics [4].

Table 14 indicates the module connector type.

Height	Type	Type
5.2 mm	TE 1565917-4	TE Connectivity

Table 14: Module Connector Type

Warning!

Only Enclustra Mars FPGA/SoC modules should be inserted into the Mars ST3 base board.

Warning!

The VCC_IO pins are directly connected to the FPGA/SoC device. Apply only compliant voltages to the VCC_IO pins; any other voltages may damage the mounted Mars FPGA/SoC module, as well as other devices on the Mars ST3 base board.

4.6 USB 3.0 Host Connector (J501)

The Mars ST3 base board is equipped with a type-A USB 3.0 host connector.

If the mounted Mars module features a USB controller, the module's high-speed (HS) USB signals are connected to J501. Depending on the mounted Mars module, super-speed (SS) USB is also supported. Details on USB connections on the board are available in Section 6.5.

Power and data signals on this connector are ESD-protected.

4.7 Micro USB 2.0 Device Connector (J500)

The Mars ST3 base board is equipped with a micro USB 2.0 device connector. This is connected to the on-board FTDI device. Please refer to Sections 6.5.2 for details.

Power and data signals on this connector are ESD-protected.

4.8 Gigabit Ethernet Port (J700)

The Mars ST3 base board is equipped with a 10/100/1000 Mbit Ethernet port. The capability of this interface depends on the connected Mars module.

The RJ45 connector with integrated magnetics is connected directly to the Mars module connector. For details on the Ethernet interface, refer to Section 6.4.

4.9 MIPI Connector (J701)

The Mars ST3 base board is equipped with a MIPI connector with two signal lanes. The signals available on this connector are routed directly to/from the FPGA banks on the SoC/FPGA device on the Mars module. Refer to Section 6.9 for details on connectivity options.

The pinout of the J701 connector corresponds to the Raspberry Pi camera pinout. In order to receive and transmit video signals through that link, FPGA support is required (video protocol implementation).

This interface is ESD-protected.

4.10 Mini DisplayPort Connector (J800)

The Mars ST3 base board is equipped with an Mini DisplayPort connector. The signals available on this connector are routed to/from the FPGA banks on the SoC/FPGA device on the Mars module. Refer to Section 6.8 for details on connectivity options.

The pinout of the J800 connector corresponds to the Mini DisplayPort standard. In order to receive and transmit video signals through the link, FPGA support is required (video protocol implementation).

This interface is ESD-protected.

4.11 HDMI Connector (J900)

The Mars ST3 base board is equipped with an HDMI connector. The signals available on this connector are routed to/from the FPGA banks on the SoC/FPGA device on the Mars module via HDMI Redriver U900. Refer to Section 6.7 for details on connectivity options.

The pinout of the J900 connector corresponds to the HDMI standard. In order to transmit video signals through the link, FPGA support is required (video protocol implementation).

This interface is ESD-protected.

4.12 microSD Card Slot (J600)

The enclosure of J600 is connected to GND.

The microSD card is connected via a level shifter to the Mars module SDIO signals.

4.13 Anios I/O Connectors IO0/IO1 (J1000/J1003)

The Anios I/O connectors can be used for custom applications: each connector provides 24 I/Os, a differential clock connection, connectivity to the I2C bus, and power supply output connections. The clock, data and I2C signals are routed to the module connector - for details, refer to the Mars ST3 Base Board User Schematics [4]. Please note that on revision 1, the designator for connector J1000 is named J1001.

Warning!

The Anios I/O pins are connected directly to the FPGA/SoC device. Use only VCC_IO voltages compliant with the equipped FPGA/SoC device; any other voltage may damage the mounted Mars FPGA/SoC module, as well as other devices on the Mars ST3 base board.

4.14 I/O Connectors IO2/IO3 (J1001/J1004)

Two I/O connectors (2 x 6) male pin headers can be used for custom applications: each connector provides 8 I/Os and 3.3 V power supply output connections.

The signals on IO2 are level shifted from VCC_IO_A on the module connector to 3.3 V on the pin header.

The signals on IO3 are level shifted as follows: the odd pins are shifted from VCC_IO_AB (i.e. the lowest voltage between VCC_IO_A and VCC_IO_B) to 3.3 V, while the even pins are shifted from VCC_CFG to 3.3 V. The even pins are shared with FTDI UART_RX/TX_LS and user LED0#, LED1#. For details, refer to the Mars ST3 Base Board User Schematics [4].

As of Mars ST3 base board revision 2, the I/O connector IO2 and IO3 are Digilent Pmod™ compatible with an IO voltage of 3.3 V.

The level shifters on I/O connectors IO2 and IO3 may limit the maximum bitrate for the affected pins. The Mars ST3 base board offers the possibility to bypass all I/O level shifters (individually per pin) if the user application requires faster bitrates or if the original unshifted voltage is desired. Please refer to the Mars ST3 Base Board User Schematics [4] for the designators of the bypass resistors and surrounding circuitry.

Please note that on revision 1, the designator for connector J1001 is named J1000.

Warning!

Valid only for Mars ST3 base board revision 1:
The I/O pins are connected directly to the FPGA/SoC device. Use only VCC_IO voltages compliant with the equipped FPGA/SoC device; any other voltage may damage the mounted Mars FPGA/SoC module, as well as other devices on the Mars ST3 base board.

Warning!

Valid only for Mars ST3 base board revision 1:
Do not insert a PMOD module to these connectors if the corresponding VCC_IO_[x] supply is not 3.3 V, as this may damage the mounted Mars FPGA/SoC module, as well as other devices on the Mars ST3 base board.

4.15 Battery Holder (J1200)

A 3 V lithium battery (CR1220) can be installed on the Mars ST3 base board for buffering the real-time clock on the connected Mars FPGA/SoC module. The battery is not included in the Mars ST3 base board.

Type	Manufacturer
FBA75002-S02B2101L	TXGA

Table 15: J1200 - Battery Holder Type

Warning!

There is a danger of explosion if the battery is replaced incorrectly - only replace the battery with the same or equivalent type recommended by Enclustra.

Used batteries should be disposed of according to the manufacturer's instructions.

4.16 FPGA JTAG Connector (J1002)

The FPGA JTAG connector allows accessing the JTAG port of the mounted Mars FPGA/SoC module. The signals on this connector are ESD protected. Series termination resistors are equipped between the module signals and the JTAG header.

Pin Number	Connection	Series Resistor
1	JTAG_TCK	22 Ω
2	JTAG_PRSNT#	-
3	JTAG_TDO	100 Ω
4	VCC_CFG	-
5	JTAG_TMS	100 Ω
6	SRST#_RDY#	100 Ω
7, 8	Not connected	
9	JTAG_TDI	100 Ω
10	GND	-

Table 16: J1002 - FPGA JTAG Connector

JTAG_PRSNT# is used to determine if an external JTAG adapter is connected; the external adapter should tie this signal to GND when plugged in. If no exteral JTAG adapter is present, JTAG_PRESNT# is pulled up and the FTDI device provides access to JTAG interface.

Warning!

The JTAG pins are connected to the FPGA/SoC device via small-value series resistors. Use only VCC_IO voltages compliant with the equipped FPGA/SoC device. Any other voltages may damage the equipped FPGA/SoC device as well as other devices on the module or Mars ST3 base board.

The JTAG connector available on the Mars ST3 base board can be used in combination with Xilinx Platform cable USB or Intel USB-Blaster download cable. For Xilinx JTAG connection, the flying wire adapter must be used. For Intel JTAG connection, the download cable can be connected directly to the on-board JTAG connector, as the pinout matches the Intel USB-Blaster pinout.

On Mars ST3 base board revision 1 the Intel JTAG adapter cannot be used because of mechanical collisions.

5 Power

5.1 Power Input

The Mars ST3 base board can be powered using one of the power input sources listed below:

- External power connection through J1301 barrel jack connector
- Internal power connection through J1300 connector

Please note that Mars ST3 base board revision 1 are using designators J1201 and J1200.

5.2 Power Generation Overview

Table 17 describes the power supplies available on the base board.

Voltage Supply Name	Voltage Value	Rated Current	Voltage Origin	Enable Signal	Power Good Signal
VCC_5V	5.0 V	4 A	Base board (VCC_MAIN)	VCC_MAIN	N/A
VCC_3V3_MOD	3.3 V	2 A	Base board (VCC_5V)	VCC_5V	PWR_EN
VCC_IO	1.8 / 2.5 V	2 A	Base board (VCC_5V)	PWR_GOOD	PWR_GOOD_IO
VCC_1V2	1.2 V	2 A	Base board (VCC_5V)	PWR_GOOD	PWR_GOOD_IO
VCC_3V3_AUX	3.3 V	0.15 A	VCC_USBD (primary voltage source) or VCC_3V3_MOD (secondary source)	VCC_USBUB / VCC_3V3_MOD	N/A

Table 17: Generated Power Supplies

VCC_OUT is a voltage input to the Mars ST3 base board coming from the Mars module.

Starting with Mars ST3 base board revision 2, the 1.2 V converter is capable of delivering an output current up to 2 A instead of 200mA.

Warning!

The maximum available output current for each voltage supply depends on your design. Make sure that the Mars module I/O banks do not draw more current than available on the output of the DC/DC converter.

5.3 Maximum Power Budget

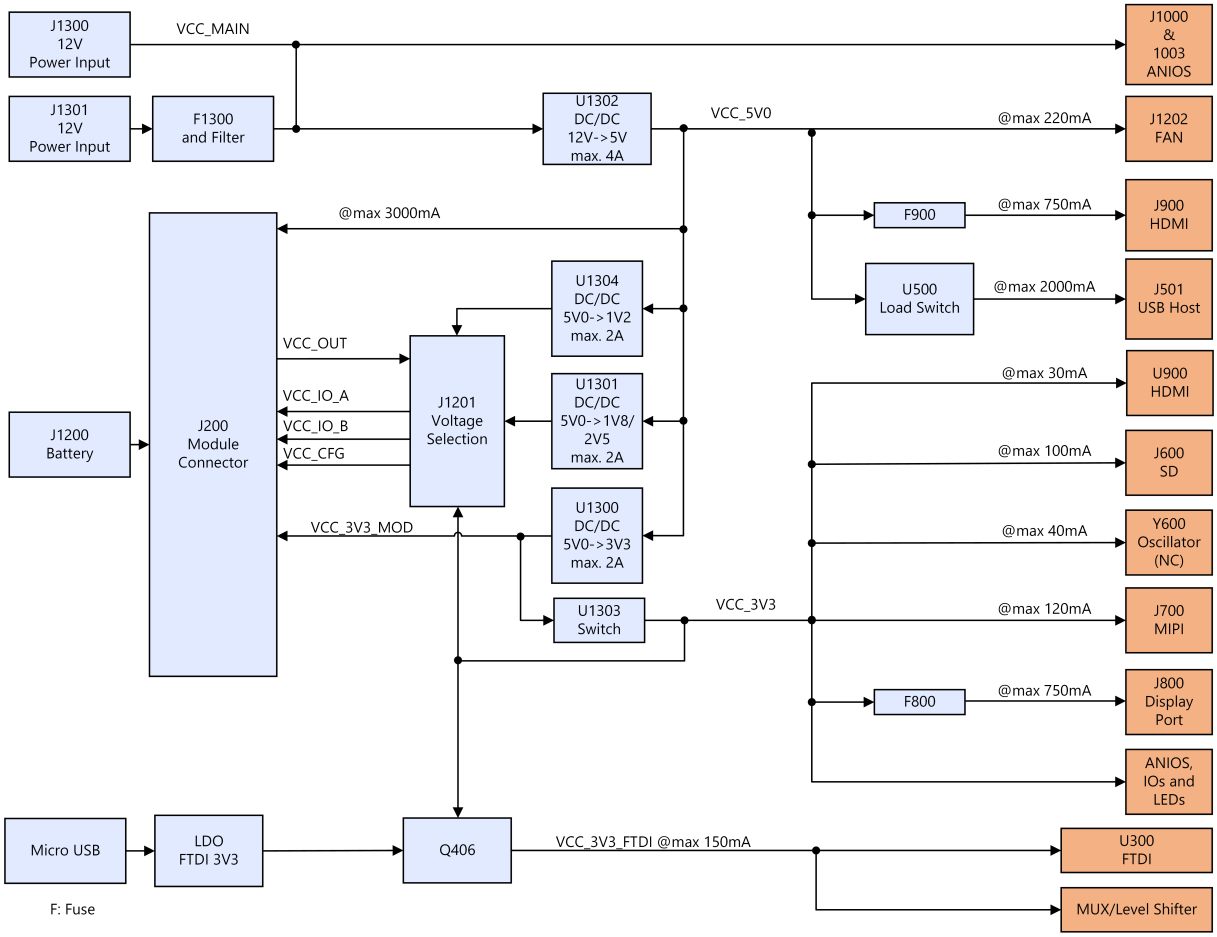


Figure 8: Maximum Power Budget Estimation

5.4 Power Sequencing

The Mars ST3 base board will only power up when a Mars module is connected to its socket.

VCC_5V and VCC_3V3_MOD voltages are generated as soon as the Mars ST3 base board is powered. These voltages are needed for powering the Mars module.

As soon as PWR_EN is asserted high, the Mars module power-up sequence is initiated. At the end of switching on the supplies on the module, VCC_OUT is up and PWR_GOOD goes high.

On the base board, the PWR_GOOD signal enables VCC_1V2, VCC_IO and VCC_3V3 and sets PWR_GOOD_IO.

A successful power-up gives access to all the bank voltage options on J1201 (on revision 1: J1104), as described in Section 4.4. If VCC_IO_A, VCC_IO_B and VCC_CFG are supplied, the green PWGD LED will turn on and indicate the end of a successful power-on sequence.

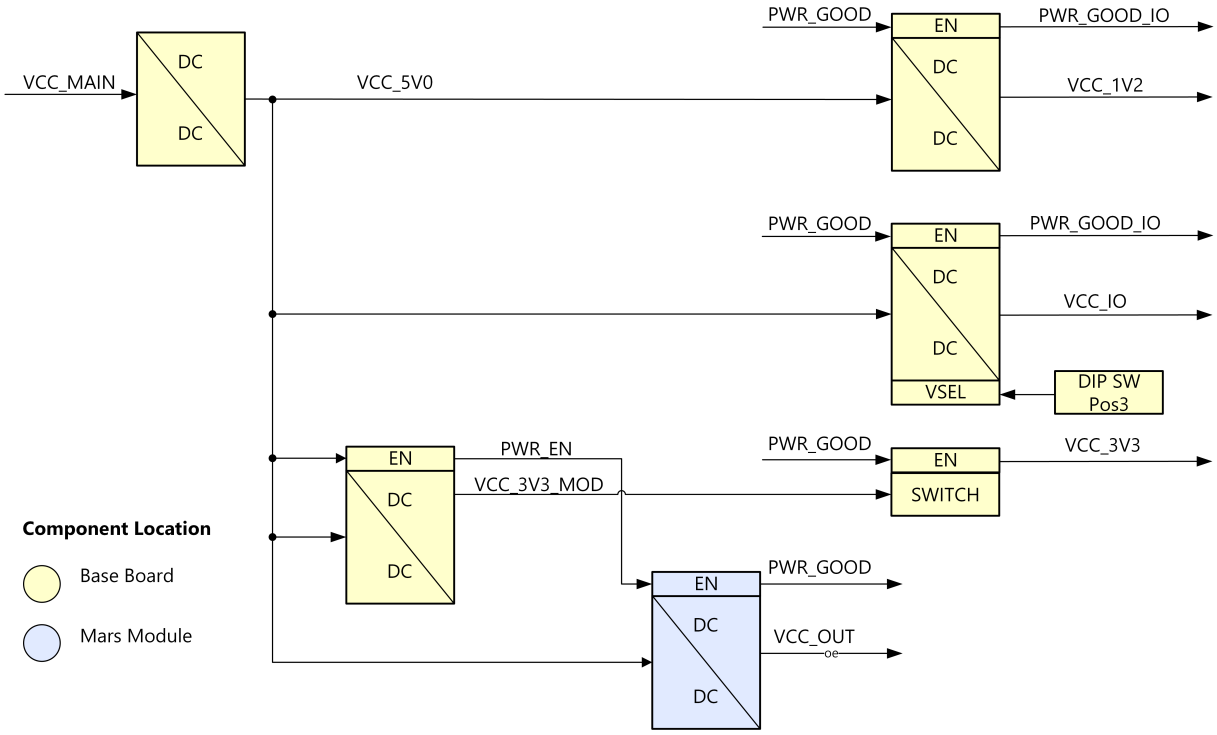


Figure 9: Power Sequence Overview

Please note that depending on the Mars module type used, the voltage level of the voltage output (VCC_OUT) may be different. Refer to the module's user manual for further information on module specific power architecture.

5.5 Power Enable/Power Good

The power enable signal, PWR_EN, may be used to shut down the DC/DC converters on the Mars module - please refer to the module's user manual for details on power generation.

On the Mars ST3 base board the VCC_5V and the VCC_3V3_MOD supplies are always active and cannot be turned-off, except by removing the 12 V power input.

The PWR_EN signal is released and no longer driven low if VCC_3V3_MOD signal is stable and 7 ms have passed since the ramp-up of VCC_5V5.

PWR_EN initiates the power sequence on the Mars module. As a result of this process, VCC_OUT is powered and PWR_GOOD is set high and available on the Mars ST3 base board.

The PWR_GOOD signal is used for enabling the bank voltage supplies located on the Mars ST3 base board - refer to Figures 9 and 10 for details.

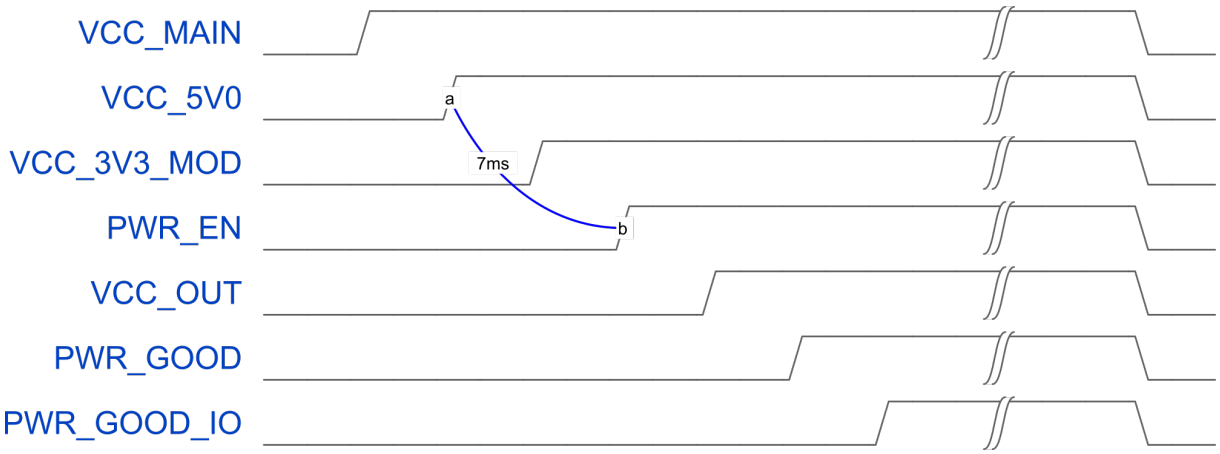


Figure 10: Power Sequence on the Mars ST3 base board with mounted Mars module

5.6 Power-Off

By removing the main supply, VCC_5V and VCC_3V3_MOD will drop. As of Mars ST3 base board revision 2, a reset circuit ensures that all converters are shut off simultaneously.

Actuator Signal Name	Off Condition	Affected Signals Pulled Low
VCC_5V	detection voltage < 3.0 V	PWR_EN, PWR_GOOD, PWR_GOOD_IO, POR#_LOAD#
PWR_EN	detection voltage < 0.8 V	PWR_GOOD, PWR_GOOD_IO, POR#_LOAD#
PWR_GOOD	detection voltage < 0.8 V	PWR_GOOD_IO, POR#_LOAD#
PWR_GOOD_IO, POR#_LOAD#_BTN	detection voltage < 0.8 V	POR#_LOAD#

Table 18: Power-Off Actuators

PWR_EN needs to be pulled low in order to perform a power cycle.

Power-on reset button is used as a reset button only. Pressing this button does not shut down any voltages nor cause a power cycle.

5.7 I/O Voltage Selection

The I/O voltage selection jumpers are used to configure VCC_IO_A, VCC_IO_B and VCC_CFG voltages that power the IO banks of the SoC/FPGA device on the mounted Mars module.

Note that on Mars ST3 base board revison 1, the VCC_IO_B must be configured from a DIP switch and not from the jumpers on the I/O voltage selection header.

The VCC_IO_A, VCC_IO_B and VCC_CFG voltages are configurable by applying the required voltage from VCC_IO, VCC_1V2, VCC_3V3, and VCC_OUT.

VCC_IO voltage is dependent on the state of the signal VSEL_IO. If VSEL_IO is low, VCC_IO is 1.8 V, otherwise VCC_IO is 2.5 V.

The selection of the voltage inputs is done by setting the I/O voltage selection jumpers and the DIP switch accordingly.

Tables 19, 21 and 20 describe the usage of jumpers. Please note the following:

- VCC_OUT is a supply output from the Mars module. The value of the voltage depends on the mounted Mars module (Refer to the "Voltage Supply Outputs" Section in the Mars module user manual).
- Only one source for each I/O voltage VCC_IO_A, VCC_IO_B or VCC_CFG is allowed.
- The factory default jumper settings are 2-4, 8-10, 11-12. As a consequence of these settings, no voltage is applied to the Mars module connector, therefore it prevents the module from booting. PWGD LED will not be lit.

Make sure that the jumper configuration chosen does not short power output nets.

The colored pins in Figure 11 represent power pins. The voltage generated on the Mars module is marked blue, while the voltages generated on the Mars ST3 base board are marked green. The grey I/O voltages pins must have a single power source.

To provide power to VCC_IO_A, VCC_IO_B and CFG pins, three jumpers are included in the product deliverables.

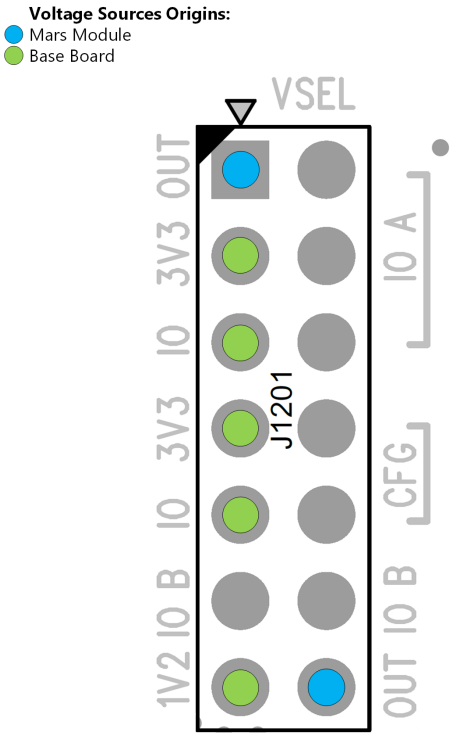


Figure 11: VCC_IO Source Pins Positions - Power Pins

Warning!

Do not merge power pins. Merging power pins can damage the Mars module or Mars ST3 base board.

Jumper Position	Source	Description
1-2	VCC_OUT	VCC_OUT is suppling VCC_IO_A
3-4	VCC_3V3	VCC_3V3 is suppling VCC_IO_A
5-6	VCC_IO	VCC_IO is suppling VCC_IO_A

Table 19: Jumper Settings VCC_IO_A

Jumper Position	Source	Description
7-8	VCC_3V3	VCC_3V3 is suppling VCC_CFG
9-10	VCC_IO	VCC_IO is suppling VCC_CFG

Table 20: Jumper Settings VCC_CFG

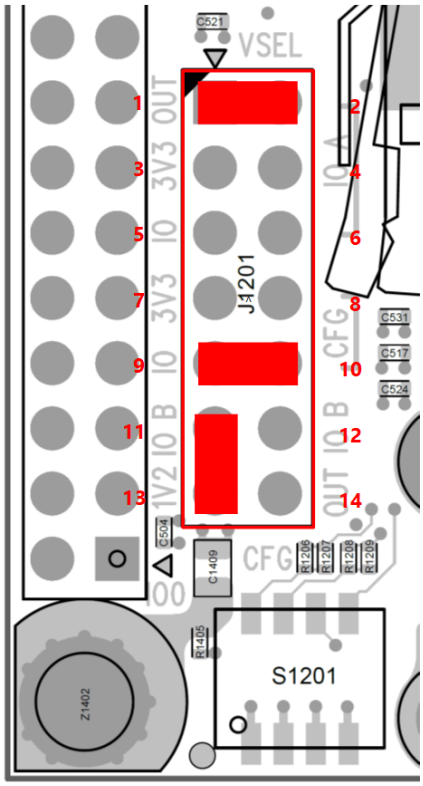
Jumper Position	Source	Description
9-11	VCC_IO	VCC_IO is suppling VCC_IO_B
11-13	VCC_1V2	VCC_1V2 is suppling VCC_IO_B
12-14	VCC_OUT	VCC_OUT is suppling VCC_IO_B

Table 21: Jumper Settings VCC_IO_B

Warning!

Use only VCC_IO_A, VCC_IO_B and CFG voltages compliant with the equipped Mars module; any other voltages may damage the interfaced Mars module, as well as other devices connected to Mars ST3 base board.

Figure 12 shows the pin numbering for connector J1201 and provides one configuration example.



Example:
VCC_IOA = VCC_OUT
VCC_IOB = 1.2 V
VCC_CFG = VCC_IO

Figure 12: VCC_IO Jumper Positions - Pin Numbering and Configuration Example

Table 22 provides information on the options for VCC_IO voltage.

VSEL_IO (CFG3 DIP switch)	VCC_IO Voltage
OFF	1.8 V
ON	2.5 V

Table 22: Voltage Options for VCC_IO

Please note that the designators of J1201 and S1201 changed from revision 1 to revision 2 boards. Furthermore, the DIP switch functionality setting VSEL_IO has migrated from CFG4 (R1) to CFG3 (R2).

6 Board Function

6.1 LEDs

LED Name	LED	Signal Name	Controlled by	Description
PWGD	D1202	PWR_GOOD	Power circuits	Indicates that PWR_GOOD is active and VCC_IO_A, B, and CFG are available
DONE	D1201	FPGA_DONE	Mars module	FPGA configuration is done
FTDI	D300	FTDI_LED	FTDI	Function controlled by the FTDI device
LED0	D1203	GPIO0_LED0#	Mars module	User LED, shared with IO connector 3 (pin 2)
LED1	D1204	GPIO1_LED1#	Mars module	User LED, shared with IO connector 3 (pin 4)

Table 23: Board LEDs

For details on the LED connections, refer to the Mars ST3 Base Board User Schematics [4].

6.2 Buttons

All buttons are active-low; their function is described in Table 24.

The user button can be configured by the user to have various functions. For details, refer to the Mars ST3 Base Board User Schematics [4].

Button Name	Button	Signal Name	Function	Comments
POR	S1200	POR#_LOAD#_BTN	Power-on reset/ Configuration-clear	Refer to the Enclustra Module Pin Connection Guidelines [8]
BTN	S1202	BTN#_WDEN#	User function	User button shared with watchdog enable

Table 24: Board Buttons

6.3 DIP Switches

There is a 4-bit configuration switch on the Mars ST3 base board. Table 25 describe its function; the factory default is marked in bold.

For details on the board configuration, refer to the Mars ST3 Base Board User Schematics [4].

DIP Switch	Signal Name	Pos.	Effect	Comments
CFG 1	BOOT_MODE0	**OFF**	**BOOT_MODE0 is set to 1**	Refer to the Mars module user manual
		ON	BOOT_MODE0 is set to 0	
CFG 2	BOOT_MODE1	**OFF**	**BOOT_MODE1 is set to 1**	Refer to the Mars module user manual
		ON	BOOT_MODE1 is set to 0	
CFG 3	VSEL_IO	**OFF**	**VSEL_IO is pulled low**	VCC_IO is set to 1.8 V
		ON	VSEL_IO is pulled to 3.3 V	VCC_IO is set to 2.5 V
CFG 4	MIPI_DSI#	**OFF**	**MIPI_DSI# is pulled to 3.3 V**	MIPI camera input
		ON	MIPI_DSI# is set low	MIPI display output

Table 25: Configuration Switch

6.4 Ethernet

The Mars ST3 base board is equipped with a Gigabit Ethernet port, configured according to the capabilities of the mounted module.

The RJ45 connector with integrated magnetics is equipped on the base board, while the Ethernet PHY is equipped on the Mars module.

6.5 USB

6.5.1 USB Overview

Figure 13 presents an overview of the USB connections on the Mars ST3 base board.

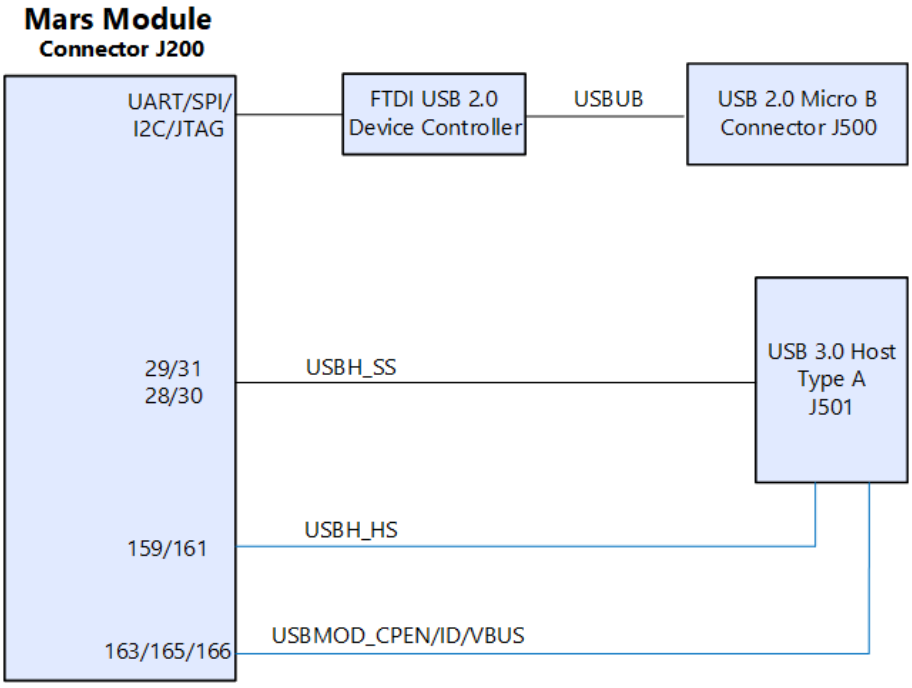


Figure 13: USB Connections Overview

USB 3.0 support is possible when the Mars module is equipped with a Zynq UltraScale+ device with USB 3.0 support on the PS GTR transceivers.

The Mars ST3 base board supports only a host connection. USB_ID is pulled to GND and the USB PHY will identify the interface as an A device. USB_CPEN controls the external VBUS power switch U500 and the switch output, VCC_USBH, is further connected to the USB PHY on the module.

The USB 2.0 micro B connector on the front panel is connected solely to the FTDI device. This connection can be used for configuration or test purposes.

6.5.2 USB 2.0 Device Controller (FTDI)

The Mars module FPGA configuration interface and QSPI flash signals are connected to the FTDI USB 2.0 device controller. This allows FPGA serial configuration and SPI flash programming over USB from a host computer without additional hardware.

Port A of the FTDI device is used for Xilinx JTAG implementation.

Port B of the FTDI is used to access the I2C bus and the UART pins of the Mars module, to program the SPI Flash or to configure the FPGA in slave serial mode. General purpose I/O pins of port B (FTDI_MODE0/1) are used to control the configuration multiplexers; refer to Table 26 for details.

By default, the UART communication between the FTDI device and FPGA is active. The Xilinx JTAG mode can be activated using the Enclustra MCT [10] and is independent of the UART connection.

The library used by the MCT is available free of charge; it allows users to integrate module enumeration, FPGA and SPI flash configuration, and I2C communication functionality in their own application. The library consists of a Windows DLL with a C-style interface, allowing use of the library from almost any programming language; for C++ applications, a C++ wrapper is also provided. Please contact Enclustra for details.

FTDI_MODE1 (BCBUS6)	FTDI_MODE0 (BCBUS5)	BOOT_MODE0 (BCBUS4)	Configuration
0	0	1	Slave serial configuration via FTDI
0	1	X	FTDI device pins connected to module I2C bus
1	0	0	SPI flash programming via FTDI
X	1	0	Master serial configuration (Mars module is configured from SPI flash)
1	1	X	FTDI device pins connected to Mars module UART pins

Table 26: FTDI Configuration Settings - Port B

The control signals FTDI_MODE0 and FTDI_MODE1 are used to configure the way BDBUS0-3 pins are routed on the module: to UART, I2C, SPI flash or Mars module SPI configuration port.

Please note that for the SPI flash programming SRST#_RDY# (BCBUS2) must be pulled low. For the slave/-passive serial configuration BOOT_MODE0 must be pulled high or left open, while for master/active serial configuration BOOT_MODE0 must be pulled low.

Warning!

After Mars module slave/passive serial configuration or SPI flash programming operations, the FTDI_MODE0 signal must be pulled high, to avoid damaging the equipped Mars module device.

6.6 I2C Communication

There are several I2C devices on the Mars ST3 base board connected to two separate I2C buses. The Mars module and the FTDI device can be I2C masters on the I2C_MGMT bus. The devices on the Mars module and the on-board Anios IO connector 1 are connected to this bus.

The I2C_USER bus is connected to the Mars module through the regular I/Os and requires an I2C controller in the FPGA logic in order to communicate with devices on the Mars ST3 base board, such as HDMI, MIPI, optional user oscillator and Anios IO connector 0. The I2C_USER bus with 0 Ω resistor jumpers to HDMI redriver and MIPI connector.

The I2C structure is illustrated in Table 27 and Figure 14. The I2C devices located on the Mars module are shown in a dashed box in Figure 14.

Please note that all I2C addresses are written in a 7-bit hexadecimal format.

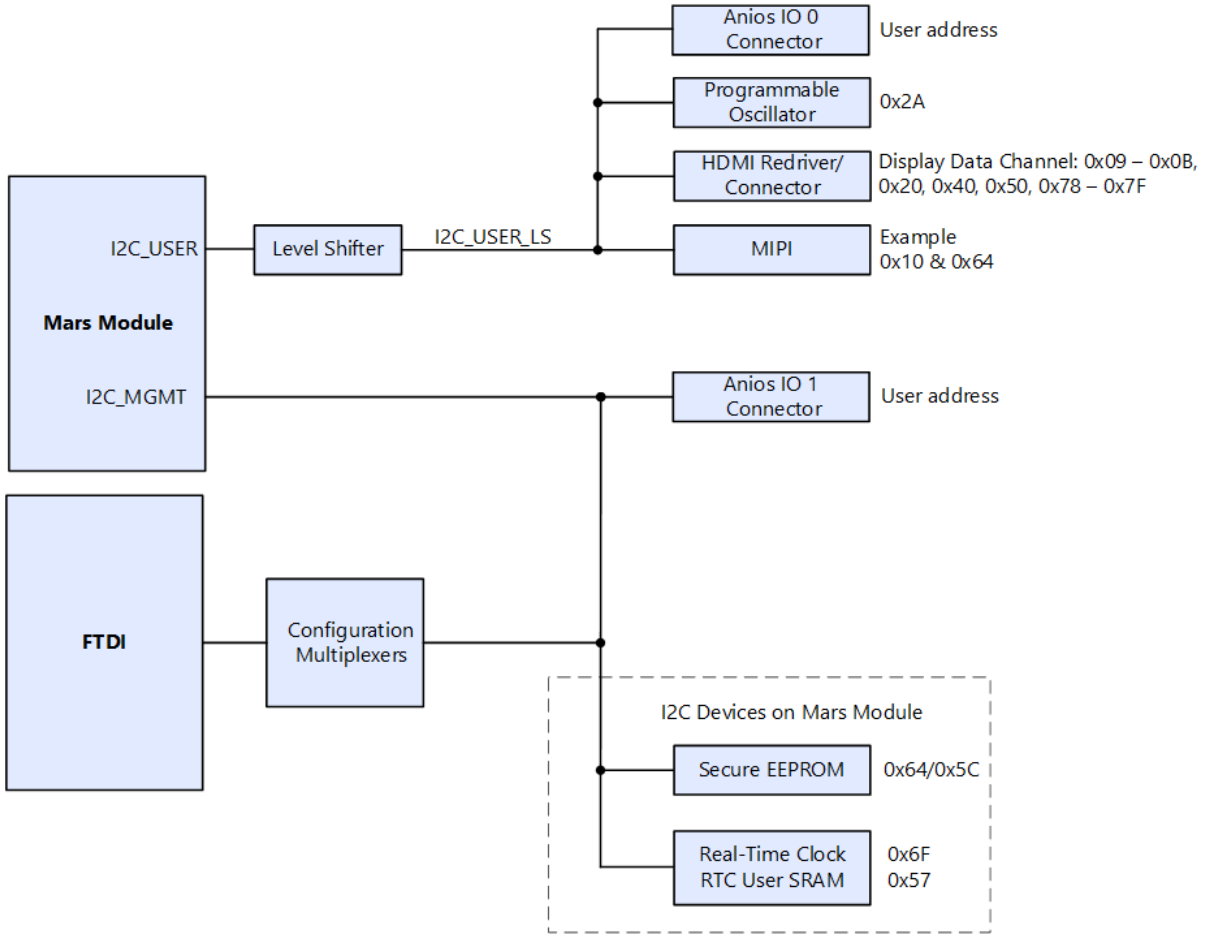


Figure 14: I2C Devices

The programmable oscillator Si570 is not equipped on the Mars ST3 base board by default, therefore the address space 0x2A is not automatically occupied.

Board Reference / Pin	I2C Net Name	Comments
J200 / 75	I2C_USER_SCL	Signal is level shifted to 3.3 V (I2C_USER_SCL_LS)
J200 / 77	I2C_USER_SDA	Signal is level shifted to 3.3 V (I2C_USER_SDA_LS)
J200 / 178	I2C_MGMT_SCL	3.3 V signal
J200 / 176	I2C_MGMT_SDA	3.3 V signal
J200 / 174	I2C_MGMT_INT#	Connected to devices on Mars module and to on-board Anios connectors
U404 / 2	I2C_MGMT_SCL	Connected to FTDI device when the FTDI mode setting is [0,1]
U404 / 5, 11	I2C_MGMT_SDA	Connected to FTDI device when the FTDI mode setting is [0,1]

Table 27: I2C Structure

6.7 HDMI

The Mars ST3 base board supports HDMI 1.4b output signals. The interface supports hot plug detect (HPD) and consumer electronics control (CEC). The display data channel (DDC) for audio and video format recognition is wired to the I2C_USER bus, controlled by the Mars module via pins 75/77 on the module connector.

The redriver equalizer configuration is done with pull-up/down resistors R920 - R923. On Mars ST3 base board revision 1, the designators of these resistors are named R906 - R911.

The three HDMI data lanes are routed to the Mars module connector pins 113/115, 119/121, 123/125, while the clock is routed to pins 109/111.

The HDMI redriver equipped on the board allows communication to DDC under a unique address 0x40.

This interface is protected against electrostatic discharge by using TVS diodes.

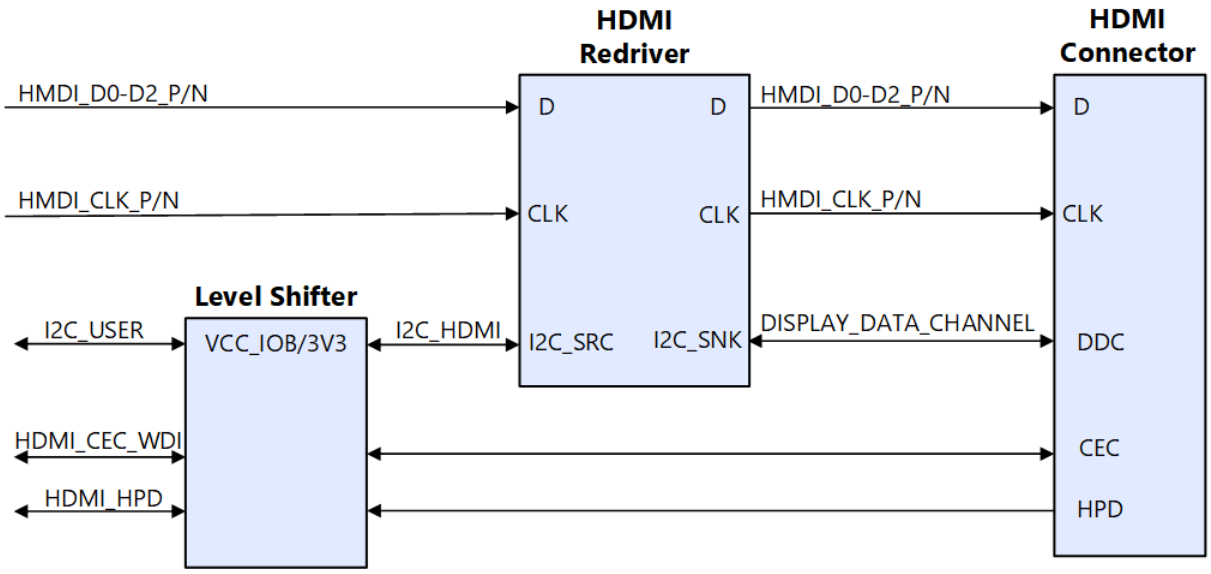


Figure 15: HDMI Connector with Redriver

6.8 DisplayPort

The Mars ST3 base board is equipped with a mini DisplayPort connector.

For DisplayPort applications the following connections are used: MGT transmitter lanes 0 (module connector pins 23/25) and 1 (pins 17/19), along with an auxiliary channel (pins 138/142/144) and a hot plug detect signal (pin 79). The translation between LVTTL and LVDS is done with a dedicated transceiver.

The supported DisplayPort standard is dependent on the connected Mars module.

This interface is protected against electrostatic discharge by using TVS diodes.

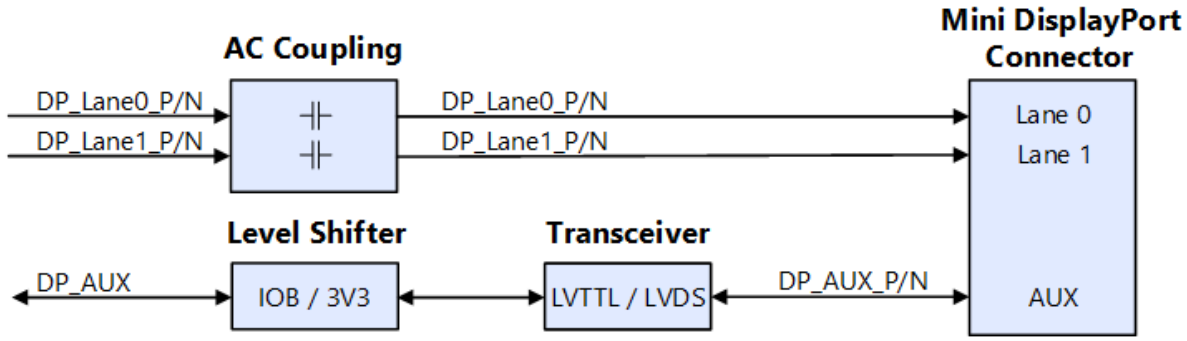


Figure 16: Mini DisplayPort Connector with LVDS Transceiver

6.9 MIPI

A MIPI (Mobile Industry Processor Interface) standard interface is available to the user. Default application supports a CSI (Camera Serial Interface) with two data lanes. The pin assignment enables the direct connection of a Raspberry Pi camera.

The MIPI pinout for CSI interface has been checked to work optimally with the Mars XU3 SoC modules. The pinout respects the RX rules indicated by the MIPI D-PHY IP core documentation [11].

Figure 17 shows the connections for the CSI use cases. When the MIPI interface is used as CSI, the USER I2C bus is used as camera control interface (CCI).

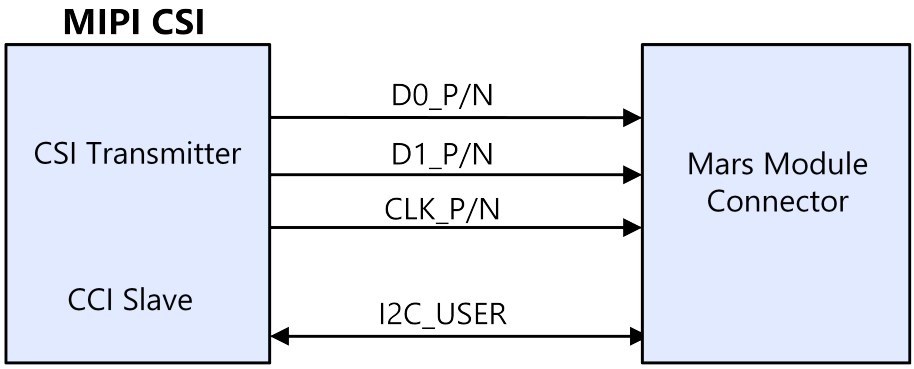


Figure 17: MIPI CSI Interface with Zynq UltraScale+ Modules

Please note that the MIPI pinout on the module connector has changed between revisions 1 and 2. Refer to the Mars ST3 Base Board User Schematics [4] and to Mars ST3 Base Board Known Issues and Changes [5] for details.

Warning!

Please note that MIPI CSI interface in combination with Zynq-7000, 7-Series (and similar Intel FPGA families), as well as MIPI DSI in combination with Zynq Ultrascale+ have not been tested on Enclustra side. The information provided further indicates the theoretical steps required for supporting these features.

For use with older FPGA families that do not natively support SLVS IO standard (Zynq-7000, 7-series, Cyclone V) hardware changes are required in order to provide proper signal termination and tap the high-speed signals to dedicated FPGA inputs. Low-power signaling is supported only for lane 0 (D0), on module connector pins 108, 110. Clock and data 1 support only the high-speed mode.

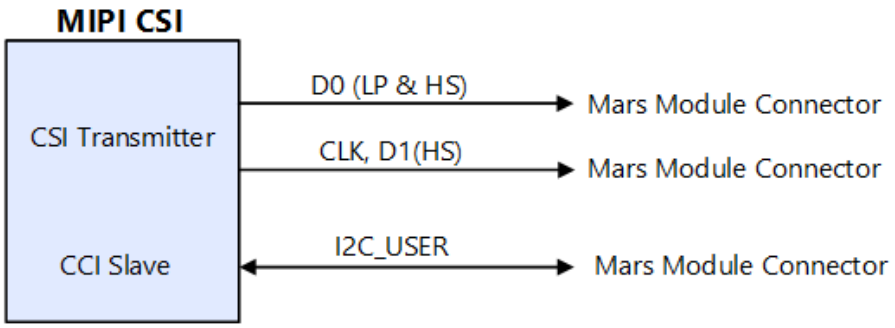


Figure 18: MIPI CSI Interface with Zynq-7000/7-Series Modules

Table 28 describes the hardware changes required to operate the MIPI CSI interfaces in combination with older FPGA families.

FPGA Family	Remove	Equip
Zynq Ultrascale+	-	-
Zynq-7000, 7-Series (and similar Intel FPGA families)	R703 - R704	R711 - R715

Table 28: MIPI Connector CSI - Hardware Changes for older FPGA Families

Starting with revision 2, it is possible to select the MIPI mode between CSI and DSI by configuring DIP switch 4 accordingly (refer to Section 6.3 for details). In DSI mode, the MIPI connector may be connected to a two-lane capable display.

If the MIPI is used in DSI mode to drive a display, mapping of clock and data lanes should be swaped according to Table 29. Please note that depending on the attached display the signal mapping may differ from the proposed permutations.

Board Reference / Pins	CSI mapping	DSI mapping
103, 105	Clock	Data Lane 0
97, 99	Data Lane 1	Clock
112, 114	Data Lane 0	Data Lane 1

Table 29: MIPI Connector CSI - Rasperry Pi Display Lane Mapping

In case of a DSI interface, the pins corresponding to I2C (in CSI mode) may be used for power - please read carefully the datasheet of the connected MIPI device to check the connectivity requirements.

6.10 User Oscillator (optional)

The Mars ST3 base board may be optionally equipped with a LVDS or LVTTL oscillator (Y600), configurable via I2C. Please refer to datasheets for proper footprint and pin assignment. Default oscillator supply voltage is 3.3 V for LVDS oscillator types. For other supply voltages, ensure that L600 and L601 are assembled accordingly.

If a I2C programmable Si570 is used, note that the oscillator is 3.3 V tolerant as the connected I2C bus signals have a voltage level of 3.3 V.

The differential clock pair is connected to the module connector pins 4/6.

6.11 Watchdog

The Mars ST3 base board features a dedicated watchdog. By default the watchdog is disconnected and does not interfere with normal operation. Once connected and enabled the watchdog can either force a power cycle or a reconfiguration of the module.

The watchdog input is a shared signal with the HMDI CEC. The resistor R916 should be removed and R917 needs to be assembled for the watchdog input to be connected. The watchdog output signal can be connected either via R611 to force a power cycle or via R612 to force a reconfiguration of the module. To enable the watchdog once power-on reset is de-asserted, resistor R623 must be assembled. To enable the watchdog once the module configuration is completed, R624 must be assembled.

Please refer to the Mars ST3 Base Board User Schematics [4] for details.

7 Operating Conditions

7.1 Absolute Maximum Ratings

Table 30 indicates the absolute maximum ratings for Mars ST3 base board.

Symbol	Description	Rating	Unit
VCC_MAIN_IN	Supply voltage relative to GND	-0.3 to 16	V
VCC_IO_[x] VCC_CFG	VCC I/O input voltage relative to GND	Refer to the Mars module user manual	
$T_{ambient}$	Ambient temperature range for wide range boards (W) *	-20 to +85	°C
$T_{storage}$	Storage temperature	-25 to +85	°C

Table 30: Absolute Maximum Ratings

7.2 Recommended Operating Conditions

Table 31 indicates the recommended operating conditions for Mars ST3 base board.

Symbol	Description	Rating	Unit
VCC_MAIN_IN	Supply voltage relative to GND	12	V
VCC_IO_[x] VCC_CFG	VCC I/O input voltage relative to GND	Refer to the Mars module user manual	
$T_{ambient}$	Ambient temperature range for wide range boards (W) *	-20 to +85	°C
$T_{storage}$	Storage temperature	-25 to +85	°C

Table 31: Recommended Operating Conditions

Warning!

** The components used on the hardware are specified for the relevant temperature range. The user must provide adequate cooling in order to keep the temperature of the components within the specified range.*

8 Ordering and Support

8.1 Ordering

Please use the Enclustra online request/order form for ordering or requesting information:
`http://www.enclustra.com/en/order/`

8.2 Support

Please follow the instructions on the Enclustra online support site:
`http://www.enclustra.com/en/support/`

List of Figures

List of Tables

References

[1] Enclustra General Business Conditions
http://www.enclustra.com/en/products/gbc/
[2] Enclustra FPGA Manager IP Solution
http://www.enclustra.com/en/products/fpga-manager/
[3] Mars ST3 Base Board IO Net Length Excel Sheet
→ Ask Enclustra for details
[4] Mars ST3 Base Board User Schematics
→ Ask Enclustra for details
[5] Mars ST3 Base Board Known Issues and Changes
→ Ask Enclustra for details
[6] Mars ST3 Base Board 3D Model (PDF)
→ Ask Enclustra for details
[7] Mars ST3 Base Board STEP 3D Model
→ Ask Enclustra for details
[8] Mercury Mars Module Pin Connection Guidelines
→ Ask Enclustra for details
[9] Mars Master Pinout
→ Ask Enclustra for details
[10] Enclustra Module Configuration Tool
http://www.enclustra.com/en/products/tools/module-configuration-tool/
[11] MIPI D-PHY v4.1, LogiCORE IP Product Guide, Vivado Design Suite, PG202, v1.4, Xilinx